MODEL
371XXA
VECTOR NETWORK ANALYZER

MAINTENANCE MANUAL

Anritsu

490 JARVIS DRIVE | MORGAN HILL, CA 95037-2809

P/N: 10410-00192
REVISION: D
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The ANRITSU product(s) listed on the title page is (are) warranted against defects in materials and workmanship for one year from the date of shipment.
ANRITSU's obligation covers repairing or replacing products which prove to be defective during the warranty period. Buyers shall prepay transportation charges for equipment returned to ANRITSU for warranty repairs. Obligation is limited to the original purchaser. ANRITSU is not liable for consequential damages.

LIMITATION OF WARRANTY

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MANUAL CHANGE

MANUAL:
Title: Model 371XXA Vector Network Analyzer Maintenance Manual
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CHANGE PACKET
Part Number: 10900-00328

Change 1, February 2001

Page E-19
Replace pages E-19 and E-20 with the enclosed like-numbered pages, Changed: February 2001.

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Appendix B — Error Codes/Messages

This appendix contains a listing of the Error Codes/Messages. Also included is a description of the information fields that are part of the error messages.

Appendix C — Connector Maintenance Check Procedures

This appendix contains procedures and information needed to perform maintenance checks (including pin-depth measurements) for the connectors on all ANRITSU supplied Calibration/Verification Kit components, Through-cables, and other associated RF/microwave components.

Appendix D — Performance Specifications

Appendix E — Millimeter Wave Instructions

This appendix provides service instructions for the 371XXA Millimeter Wave System. The information is peculiar to the the 371XXA and is intended to supplement the common service instructions contained in the other parts of this manual.

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Chapter 3 Operational Tests

Chapter 4 Performance Verification

Chapter 5 Troubleshooting

Chapter 6 Adjustments

Chapter 7 System Description

Chapter 8 Remove and Replace Procedures

Chapter 1
General Information

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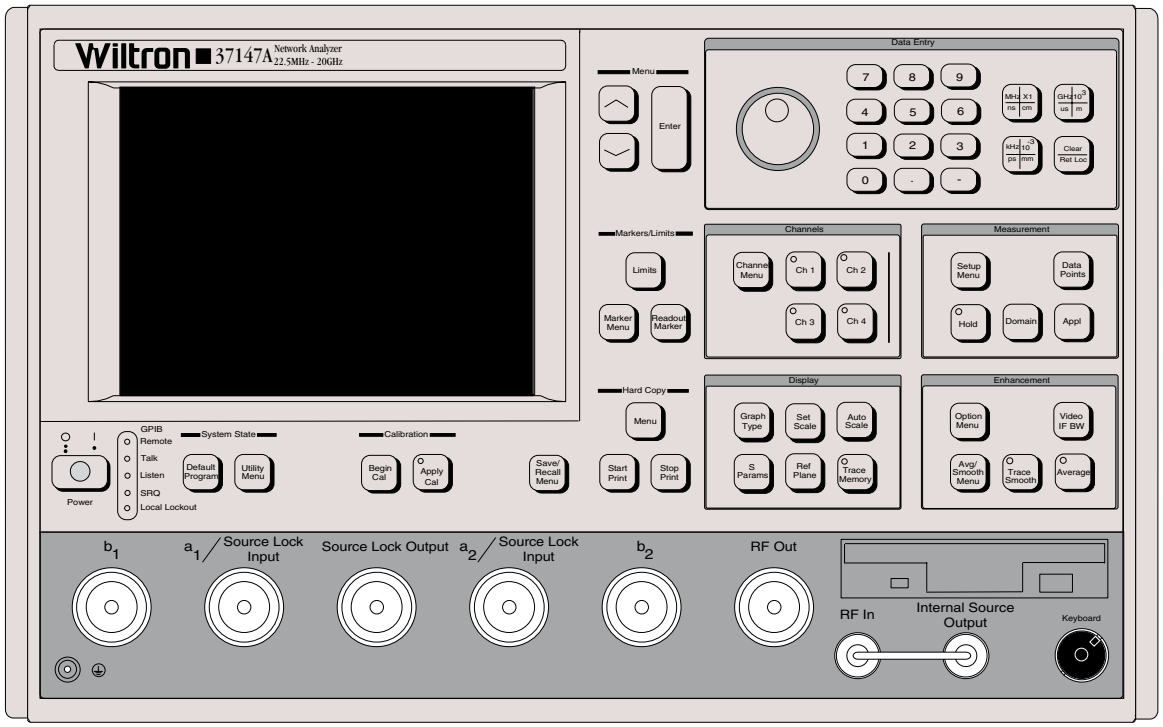


Figure 1-1. *Series 37100A Vector Network Analyzer System*

Chapter 1
General Information

1-1 SCOPE OF MANUAL

This manual provides general service and preventive maintenance information for the ANRITSU 371XXA family of Vector Network Analyzer (VNA) systems. It contains procedures for:

- Testing the instrument for proper operation.
- Verifying measurement accuracy and traceability to National Institute of Standards and Technology (NIST).
- Troubleshooting a failed instrument to the exchange subassembly level or the subsystem requiring adjustment.
- Adjusting instrument internal sub-systems.
- Locating and replacing failed parts

Throughout this manual, the terms "371XXA" and "371XXA VNA" will be used interchangeably to refer to all Series 37100A Network Analyzer system models, unless otherwise noted.

1-2 INTRODUCTION

This chapter of the manual provides a general description of 371XXA VNA systems, system serial numbers, frequency ranges, and related manuals. Also included is information about the level of maintenance covered in this manual, service strategy, available service facilities, and static-sensitive component handling precautions. A list of recommended test equipment is also provided.

1-3 ONLINE MANUALS

This manual is available on CD ROM as an Adobe Acrobat™ (*.pdf) file. The file can be viewed using Acrobat Reader™, a free program that is also available on the CD ROM. This file is "linked" such that the viewer can choose a topic to view from the displayed "bookmark" list and "jump" to the manual page on which the topic resides. The text can also be word-searched. CD ROM part numbers are available on ANRITSU's Internet home page (http://www.global.anritsu.com). You can also contact ANRITSU Customer Service for price and availability

1-4 IDENTIFICATION NUMBER

All ANRITSU instruments are assigned a six-digit ID number, such as "401001". This number appears on a decal affixed to the rear panel. Please use this identification number during any correspondence with ANRITSU Customer Service about this instrument.

1-5 SYSTEM DESCRIPTION

371XXA Model Frequencies

Model	Freq Range
37147A	22.5 MHz to 20.0 GHz
37169A	22.5 MHz to 40.0 GHz

The 371XXA Analyzers are microprocessor controlled Vector Network Analyzers. Each is a single-instrument system that contains a built-in signal source, a test set, and an analyzer subsystem. A typical model (37169A) is shown in Figure 1-1. These analyzers are produced in two models that cover a range of from 22.5 MHz to 40 GHz. The table at left lists the frequencies for each model.

1-6 RELATED MANUALS

The 371XXA Vector Network Analyzer Operation Manual (10410-00149) describes the front panel operation for all 371XXA models. It also contains general information, specifications, and Performance Verification procedures for all models.

The 371XXA Series Vector Network Analyzer Programming Manual (10410-00160) describes all 371XXA GPIB commands and provides programming information for operation of the 371XXA remotely via the IEEE-488 General Purpose Interface Bus. Included at the rear of this manual is the 371XXA Series Vector Network Analyzer GPIB Quick Reference Guide (10410-00164).

1-7 STANDARD OPTIONS

The standard 371XXA VNA options and their respective Upgrade Kit part numbers are:

Option*	Description	Upgrade Kit
Opt 1	Rack Mount w/slides	ND39486
Opt 1A	Rack Mount	ND40916
Opt 2A	Time Domain (Microwave Units)	ND39477
Opt 10A	High Stability Ovenized Time Base, 1 Hz Frequency Resolution	ND45045

* All options listed can be installed at ANRITSU Service Centers

1-8 SERVICE STRATEGY

This paragraph provides an overview of the 371XXA VNA service strategy and available service facilities. It also provides references to the information in various locations in this manual needed to accomplish the service functions required for the 371XXA VNA.

Appendices - Refer to the Appendices at the rear of this manual for detailed descriptions of the following:

- Diagnostics Menus and GPIB Commands.
- Error Messages.

Functional Assembly Level Troubleshooting

The 371XXA modular design, extensive built-in diagnostics, and automated service tools are designed to support fast exchange of functional assembly level repairs.

Failed assemblies are not field repairable. Once an assembly is found to be faulty, it should be returned to an authorized ANRITSU Service Center for exchange. Refer to the description of the Exchange Assembly Program in Chapter 2, Replaceable Parts.

The procedures for troubleshooting a failed 371XXA VNA are described in this manual in Chapter 5, Troubleshooting.

Internal Hardware Adjustments and Calibrations

There are four automated internal hardware field calibrations. Two of them are used to characterize the 371XXA frequency and power generation sub-systems. These calibrations insure fast, consistent phase lock of system frequencies and proper compensation, leveling, and flatness of system power at the front panel test ports.

To conduct these calibrations, you need only connect the appropriate test equipment (counter or power meter) to the 371XXA and initiate the calibration. The 371XXA will control itself and the externally connected test equipment to perform measurements and store calibration constants in its internal battery backed RAM (BBRAM).

The procedures for adjusting the 371XXA VNA are described in this manual in Chapter 6, Adjustments.

Internal Service Log

The 371XXA continuously monitors itself for proper operation. Should a failure occur, it notifies the user via a failure message on the display screen. (In remote-only operation, it also sets the GPIB Status Byte, if enabled.) It also writes the error message along with some data pertinent to the failure to an internal service log stored in battery-backed memory.

The service log can be checked at any time to view (without erasing) all error messages that were written into it. It is capable of storing more than 30 pages of service messages and data. The 371XXA will automatically remove the oldest errors first to make room for new errors, if necessary. To check the contents of the service log, use the procedure described in Chapter 3, Operational Tests.

NOTE

A printed or disk file copy of the Service Log (with the failure in question) must be made available to ANRITSU when exchanging a failed assembly, or when requesting service support. Refer to Chapter 2, Replaceable Parts, for further information.

System Test/ Certification

Quick operational checkout of the system may be accomplished by the system user or for incoming inspection purposes using the “Operational Checkout” chapter in the 371XXA Operations Manual. Those procedures

are useful in quickly verifying that the instrument's primary measurement functions are operational and stable.

Full operational testing of the system is detailed in Chapter 3, Operational Tests. These tests should be performed annually, or more often depending on system use.

Verification of the system's measurement accuracy and other key performance parameters may be done using the procedures in Chapter 4, Performance Verification. This should be performed annually, or more often depending on system use.

Preventive Service

The 371XXA A9 Processor PCB contains a battery-backed memory/real time clock chip (BBRAM) and a static memory (SRAM) backup battery. These have a finite life span and should be replaced periodically per the procedures in Chapter 8, Removal and Replacement Procedures.

The BBRAM chip has a rated life span of 4 years. The SRAM backup battery has a worst case elapsed time for SRAM battery protection of 200 days. The SRAM battery life span will vary according to how the system is used; that is, how often the system is powered off for extended periods of time.

Servicing Specially Modified Instruments

Instruments with customer requested special modifications performed by ANRITSU will have an identifying Specials Modification number printed on the rear panel. This number will be preceded with the letters SM, i.e., SM1234 is special modification number 1234.

Special instruments may have service requirements different from those specified in this manual. Contact your local Service Center if you need more information when servicing such instruments.

1-9 SERVICE SUPPORT INFORMATION

The following paragraphs briefly describe the various service support services and aids available to you to help you maintain your 371XXA.

Technical Support

Technical service support is available by contacting any ANRITSU Worldwide Service Center (see Chapter 2). Or, service support may be obtained directly from the factory by contacting:

ANRITSU Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)778-2000
FAX: (408)778-0239

If servicing or repairing your own system and you need technical support, you will need to FAX or mail a printout of the items listed below to the ANRITSU Customer Support Engineer:

- Measurement data in question
- "Operational Tests" results
- System state (from UTILITY menu)
- Service Log (from DIAGNOSTICS menu)

Service Software

The service software listed below is contained on the diskette located at the rear of this manual:

ANRITSU 37XXX Test Software (2300-178).
This software contains a series of automated tests designed to insure the 371XXA signal paths are functioning properly and capable of supporting stable calibrations and measurements. See Operational Tests Chapter for details.

Test Fixtures/ Aids

The test fixtures and test aids listed below are available through your local ANRITSU Sales or Service Center:

Rear Panel Printer Port Test Fixture (B39553).
This test fixture is used to check out digital printer interface circuits on the rear panel assembly.

GPIB Cable (2100-2).
This cable is used to check out digital GPIB interface circuits on the rear panel assembly.

Front Panel Source Lock Test Fixture (ND45331).
This test fixture is used to evaluate system performance.

Front Panel Source Lock Test Fixture (ND45332).
This test fixture is used to evaluate system performance.

Failed Assembly Exchange Program

The exchange program allows a customer to quickly exchange a failed subassembly for a factory refurbished, fully system-tested end unit that is under warranty. This results in significant time and price savings as compared with ordering a new assembly.

Refer to Chapter 2, Replaceable Parts, for a complete list of exchangeable assemblies for all Series 37100A models.

NOTE

When sending a failed assembly to the factory for exchange, a copy of the Service Log **must always** accompany the failed assembly. Refer to Chapter 2, Replaceable Parts, for further information.

1-10 RECOMMENDED TEST EQUIPMENT

Table 1-1 lists the recommended test equipment to be used for all maintenance activities for all Series 37100A models. Note the "Use" codes listed in the right hand column of the table. These codes list the applicable maintenance activities for the equipment listed.

Table 1-1. *Recommended Test Equipment (1 of 1)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USE**
Computer/Controller	Equipped with National Instruments GPIB Interface Adapter, w/Driver Software V2.1 or later	ANRITSU 360CC or 360CC-2, with a PCII/IIA, or, ANRITSU 360CC-3 and RS-232/GPIB-US (or -UK/ -EU)	O, P
Test Software		ANRITSU 2300-178	O
Floppy Disk	Formatted, IBM PC format	DS/HD 1.44 Mbyte	A
GPIB Cable		ANRITSU 2100-2, or equivalent	O, P, A
RF/Microwave Cable	DC – 40 GHz, K type connectors (male or female), Length, 3 ft.	Any	P, A
BNC Cable	Length, 4 ft., 2 each	Any	O
Printer Port Test Fixture		ANRITSU B39553	O
Source Lock Out Signal Divider		ANRITSU ND45331	O, P
RF Out Signal Divider		ANRITSU ND45332	O, P
Fixed Attenuator	Contains test data	ANRITSU 41KC-10, w/Opt C	P
Fixed Attenuator		ANRITSU 41KC-3	P
Thru Line		ANRITSU 3670K50-2, 3671K50-2	O
Calibration Kit		ANRITSU 3652-1*	O, P
Frequency Counter	*Frequency:* 0.1 to 26.5 GHz *Input Impedance*: 50Ω	EIP Microwave, Inc., Model 578B	P, A
Digital Multimeter	*Resolution:* 4½ digits *DC Accuracy:* 0.1 % *AC Accuracy:* 0.1 %	Any	T
Oscilloscope	*Bandwidth:* DC to 100 MHz *Sensitivity:* 2 mV *Horiz. Sensitivity:* 50 ns/division	Tektronix, Inc. Model 2445	T
Power Meter 1, with: Power Sensor 1 ***or:*** Power Meter 2, with: Power Sensor 2	*Power Range:* –30 to +20 dBm (1 mW to 100 mW) *Other:* GPIB controllable *Frequency Range:* 0.05 to 50 GHz *Power Range:* –70 to +47 dBm (100 pW to 50 W) *Other:* GPIB controllable *Frequency Range:* 0.01 to 40 GHz	Anritsu Model ML24xxA Power Meter MA2425A/b Gigatronics 8541 or 8542 Gigatronics 80304A	P, A P, A
Gauging Set	GPC-7 Gauging Set K Connector Gauging Set	ANRITSU 01-161 ANRITSU 01-162	O, T

** USE CODES:
- A Adjustment / Internal Hardware Calibration
- O Operational Testing
- P Performance Verification
- T Troubleshooting

* Calibration Kit sliding load (Option {-1}), required for Performance Verification only.

1-11 STATIC SENSITIVE COMPONENT HANDLING PROCEDURES

The 371XXA contains components that can be damaged by static electricity. Figure 1-2 (next page) illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

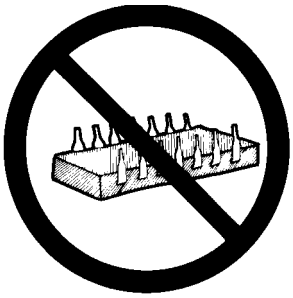
1-12 SERVICE CENTERS

ANRITSU Company offers a full range of repair and calibration services at fully staffed and equipped service centers throughout the world. Table 2-1, located on page 2-4, lists all ANRITSU service centers.

1-13 PERFORMANCE SPECIFICATIONS

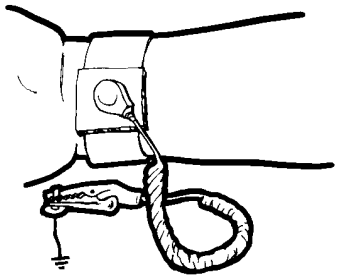
The performance specifications for all Series 371XXA models are contained in the Technical Data Sheets that are located in Appendix D, Performance Specifications.

1. Do not touch exposed contacts on any static sensitive component.



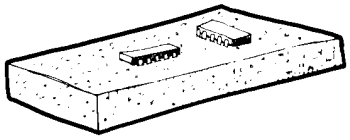
2. Do not slide static sensitive component across any surface.

3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

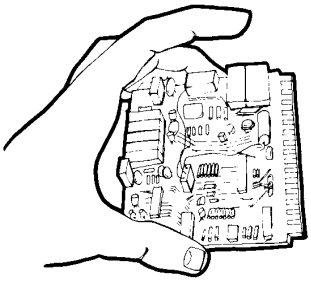


4. Wear a static-discharge wristband when working with static sensitive components.

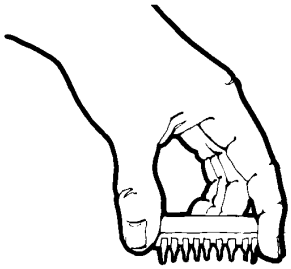
5. Label all static sensitive devices.



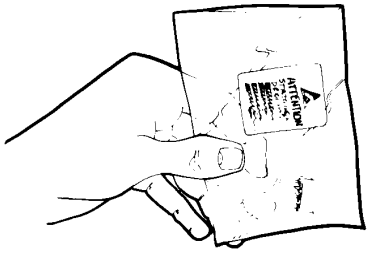
6. Keep component leads shorted together whenever possible.



7. Handle PCBs only by their edges. Do not handle by the edge connectors.



8. Lift & handle solid state devices by their bodies – never by their leads.



9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 1-2. *Static Sensitive Component Handling Procedures*

Chapter 2
Replaceable Parts

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Chapter 2
Replaceable Parts

2-1 INTRODUCTION

This chapter provides replaceable parts information for all 371XXA models. The major replaceable 371XXA assemblies and parts are listed in Tables 2-2 through 2-7. The locations of these assemblies/parts are shown in Figures 2-1 through 2-3.

2-2 EXCHANGE ASSEMBLY PROGRAM

ANRITSU maintains a module exchange program for selected subassemblies. If a malfunction occurs in one of these subassemblies, the defective item can be exchanged. Upon receiving your request, ANRITSU will ship the exchange subassembly to you, typically within 24 hours. You then have 45 days in which to return the defective item. All exchange subassemblies or RF assemblies are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

NOTE

When sending a failed assembly to the factory for exchange, a copy of the Service Log **must always** accompany the failed assembly. This copy may be a printout, or a saved disk copy. Due to the importance of the service log information to the ANRITSU factory Service Engineers, the exchange prices are only valid if the service log data is included with the failed assembly.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local sales representative or call ANRITSU Customer Service direct (refer to paragraph 2-4.

2-3 REPLACEABLE SUBASSEMBLIES AND PARTS

Tables 2-2 through 2-5, (starting page 2-5) list the major replaceable subassemblies and parts for the 371XXA. These assemblies/parts are presently covered by the ANRITSU exchange assembly program. Table 2-6 (page 2-6) lists disposable parts for the 371XXA, and Table 2-7 lists factory-repairable parts for the 371XXA. (The parts listed in Tables 2-6 and 2-7 are not presently on the exchange assembly program.)

NOTE

The 371XXA A17 Motherboard PCB Assembly is not a field-replaceable item.

2-4 PARTS ORDERING INFORMATION

All parts listed in Tables 2-2 through 2-7 may be ordered from your local ANRITSU service center (Table 2-1). Or, they may be ordered directly from the factory at the following address:

ANRITSU Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

Table 2-1. *ANRITSU Service Centers*

UNITED STATES

ANRITSU COMPANY
490 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 778-2000
FAX: (408) 778-0239

ANRITSU ANRITSU COMPANY
685 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 776-8300
FAX: (408) 776-1744

ANRITSU ANRITSU COMPANY
10 Kingsbridge Road
Fairfield, NJ 07004
Telephone: (201) 227-8999
FAX: (201) 575-0092

AUSTRALIA

ANRITSU PTY. LTD.
Level 2, 410 Church Street
North Parramatta
NSW 2151 Australia
Telephone: 026-30-81-66
Fax: 026-83-68-84

BRAZIL

ANRITSU ANRITSU ELECTRONICA LTDA.
Praia de Botafogo, 440-SL 2401-Botafogo
2225-Rio de Janeiro-RJ-Brasil
Telephone: 021-28-69-141
Fax: 021-53-71-456

CANADA

ANRITSU ANRITSU INSTRUMENTS LTD.
215 Stafford Road, Unit 102
Nepean, Ontario K2H 9C1
Telephone: (613) 828-4090
FAX: (613) 828-5400

CHINA

ANRITSU BEIJING SERVICE CENTER
416W Beijing Fortune Building
5 Dong San Huan Bei Lu
Chao Yang Qu, Beijing 100004, China
Telephone: 86-1-50-17-559
FAX: 86-1-50-17-558

FRANCE

ANRITSU ANRITSU S.A
9 Avenue du Quebec
Zone de Courtaboeuf
91951 Les Ulis Cedex
Telephone: 016-44-66-546
FAX: 016-44-61-065

GERMANY

ANRITSU ANRITSU GmbH
Rudolf Diesel Strabe 17
8031 Gilching
Telephone: 08-10-58-055
FAX: 08-10-51-700

INDIA

MEERA AGENCIES (P) LTD.
A-23 Hauz Khas
New Delhi 110 016
Telephone: 011-685-3959
FAX: 011-686-6720

ISRAEL

TECH-CENT, LTD
Haarad St. No. 7, Ramat Haahayal
Tel-Aviv 69701
Telephone: (03) 64-78-563
FAX: (03) 64-78-334

ITALY

ANRITSU ANRITSU Sp.A
Roma Office
Via E. Vittorini, 129
00144 Roma EUR
Telephone: (06) 50-22-666
FAX: (06) 50-22-4252

JAPAN

ANRITSU CORPORATION
1800 Onna Atsugi-shi
Kanagawa-Prf. 243 Japan
Telephone: 0462-23-1111
FAX: 0462-25-8379

KOREA

ANRITSU CORPORATION
#2103 Korea World Trade Center
159-1 Samsung-Dong
Kangnam-ku, Seoul
Telephone: (02) 551-2250
FAX: (02) 551-4941

SINGAPORE

ANRITSU ANRITSU (SINGAPORE) PTE LTD
3 Shenton Way #24-03
Shenton House
Singapore 0106
Telephone: 011-65-2265206
FAX: 011-65-2265207

SWEDEN

ANRITSU ANRITSU AB
Box 247
S-127 25 Skarholmen
Telephone: (08) 74-05-840
FAX: (08) 71-09-960

TAIWAN

ANRITSU CO., LTD.
8F, No. 96, Section 3
Chien Kuo N. Road
Taipei, Taiwan, R.O.C.
Telephone: (02) 515-6050
FAX: (02) 509-5519

UNITED KINGDOM

ANRITSU ANRITSU LTD.
200 Capability Green
Luton, Bedfordshire
LU1 3LU, England
Telephone: 05-82-41-88-53
FAX: 05-82-31-303

Table 2-2. *Printed Circuit Board Assemblies**

Reference Designator	371XXA Option	Assembly / Part	Part Number
A1		LO1	D46866-3
A2		LO2	D41157-3
A3		Test A IF	D38503-4
A4		Reference IF	D41794-3
A5		A/D	D38505-3
A6		Test B IF	D38503-5
A7		LO3	D38507-3
A7	Opt 10	LO3	D38507-4
A8		Source Lock/ Separation Control	D47488-3
A9		Main Processor	B38509
A13		I/O #1	D38513-3
A14		I/O #2	D38514-3
A15		Graphics Processor	D44281-3
A16		Hard Disk (w/ PCB)	D41041-3
A18		Rear Panel PCB	D44255-3
A19**		Front Panel Switch PCB	P/O ND44610
A20**		Front Panel Control PCB	P/O ND44610
A21A1		Source YIG/Bias Control (p/o Signal Source Module)	D485161-3
A21A2		Source Control (p/o Signal Source Module)	D41841-3
A24		VME Bus Terminator	D38524-3

* These PCB assemblies are used for all models of ANRITSU Series 37100A VNA systems.
** These PCB's are part of the Front Panel Assembly (refer to Table 2-5).

Table 2-3. *Test Set Assembly RF / Microwave Components (1 of 2)*

Assembly / Part	371XXA Model / Option	Part Number
Level Detector	All	C24950-2
Power Amplifier	All	D25035-1
20 GHz Quad Buffer Amp/Sampler	37147A only	D44364
40 GHz Quad Buffer Amp/Sampler	37169A only	D44364
Switched Doubler Module (SDM)	37169A only	D28540
6 dB Pad	37169A only	43KC-3

Table 2-4. *Signal Source Module RF / Microwave Components*

Assembly / Part	371XXA Model / Option	Part Number
YIG Oscillator (2 - 20 GHz)	All	C21620-1
Down Converter	All	D27532
Switched Filter	All	D45243

Table 2-5. *Miscellaneous /Integrated Assemblies*

Assembly / Part	371XXA Model / Option	Part Number
10 MHz Ovenized Oscillator	Opt 10 only	ND39476
Power Supply Module	All	40-116
VGA Monitor	All	2000-322
Floppy Disk Assy	All	C38550
Front Panel Assy (w/ Front Panel, A19 and A20 PCB's, and all Model ID Overlays)	All	ND44610
Fan Assembly, Rear Panel	All	B38533
LCD Assembly	All	15-92

Table 2-6. *Consummsable Parts*

Assembly / Part	371XXA Model / Option	Part Number
System Software	All	2300-212
Front Panel Encoder Knob	All	2000-577
Front Panel Amber Lens	All	790-412
Fuse, 8A, Fast Blow 3AG Cartridge type (F1 Line fuse for power supply assembly)	All	631-72
Battery Backed RAM	All	54-1350
Back-Up Battery	All	633-20
LCD Backlight Lamp	All	632-55

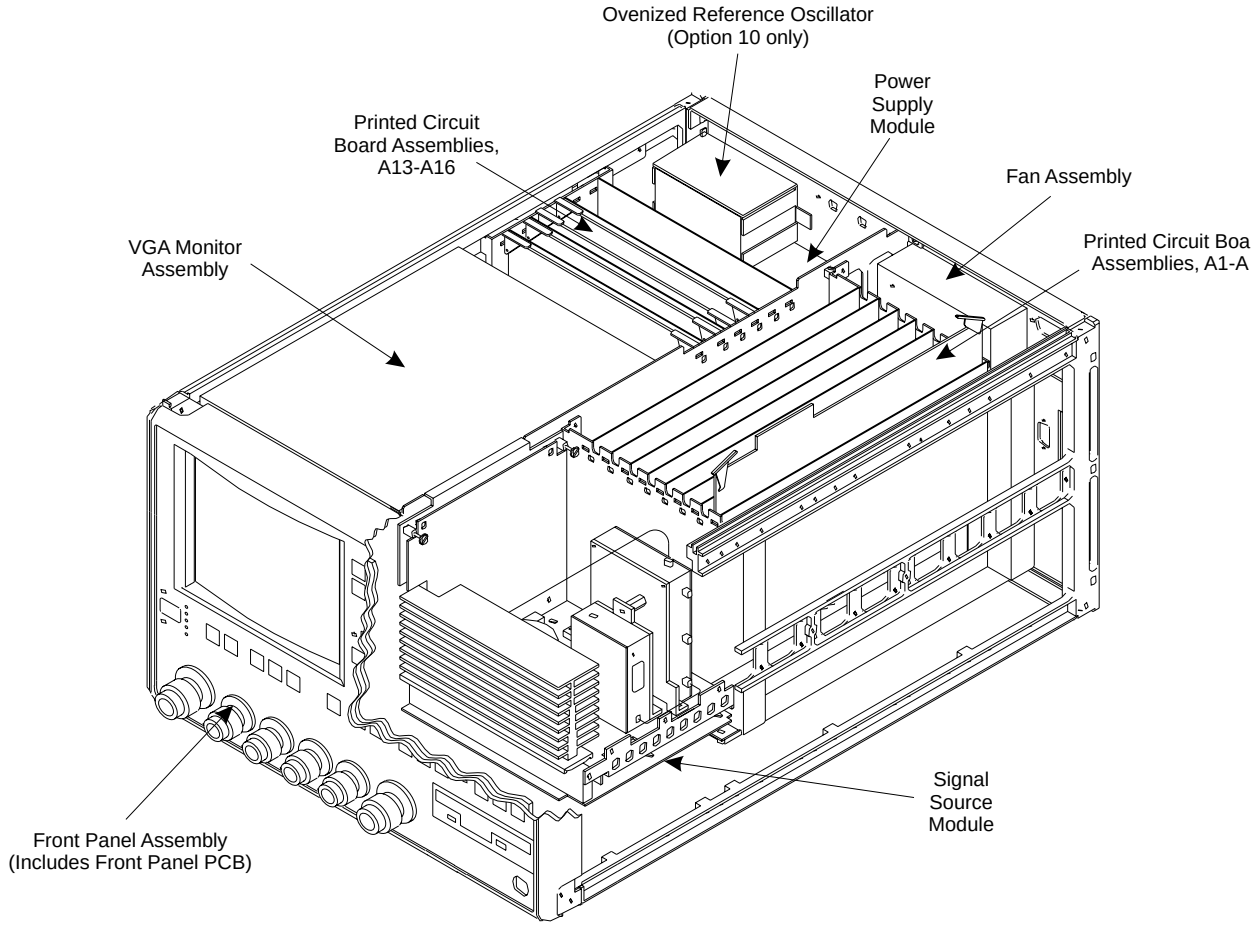

Figure 2-1. 371XXA Major Assemblies Location Diagram (Top ¾ View)

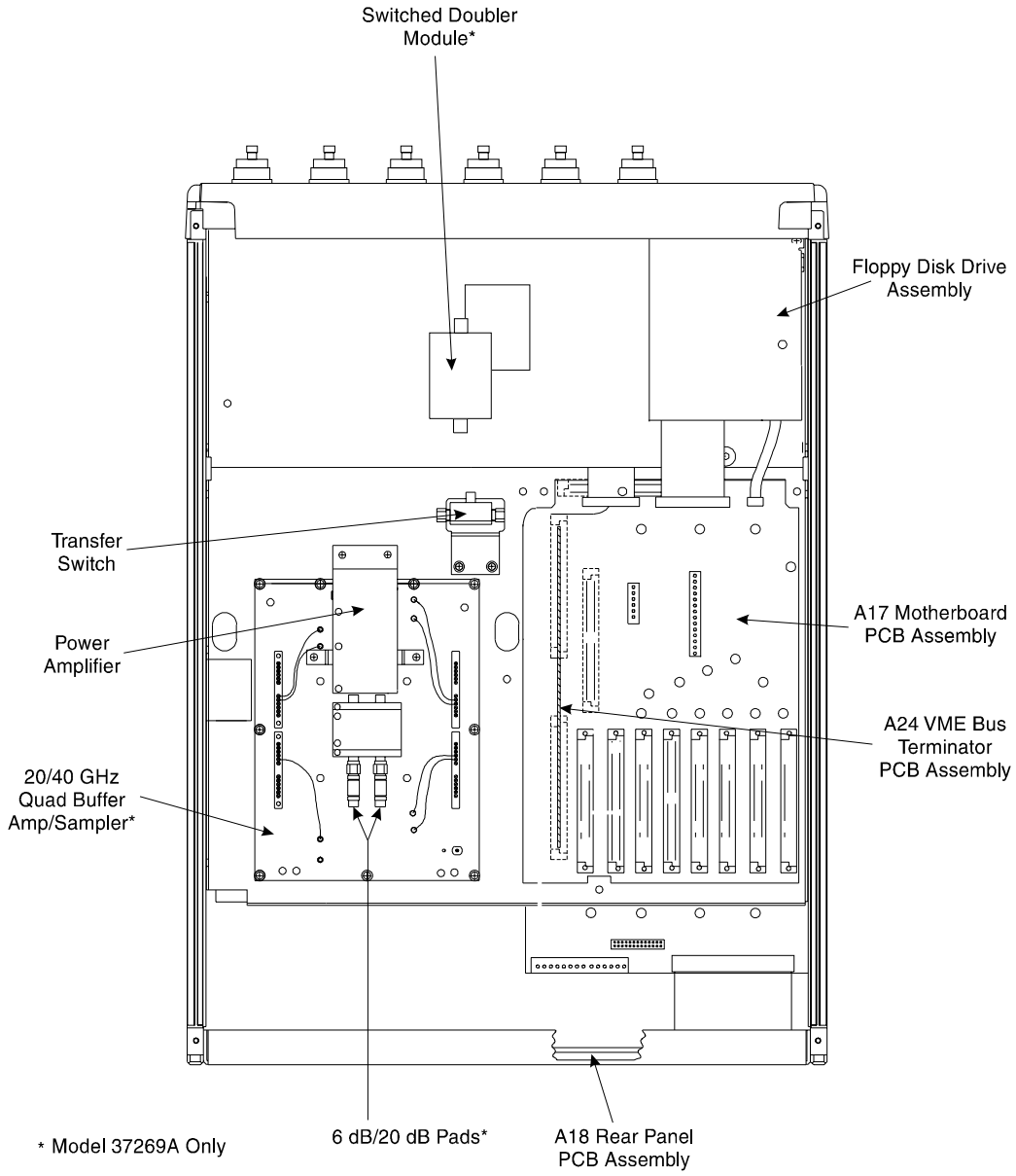

Figure 2-2. *371XXA Major Assemblies Location Diagram (Bottom View)*

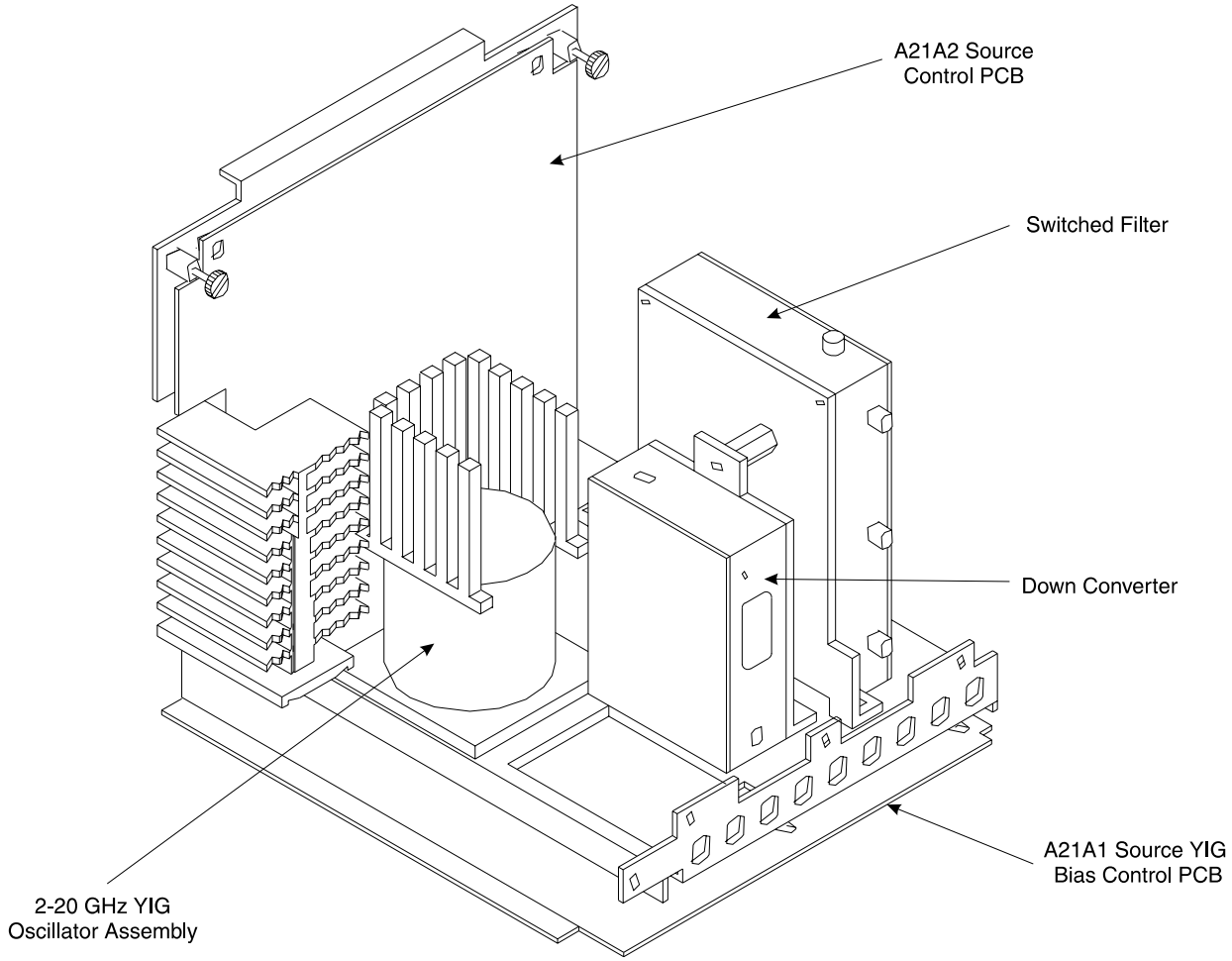

Figure 2-3. *Signal Source Parts Location Diagram*

Chapter 3
Operational Tests

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Chapter 3
Operational Tests

3-1 INTRODUCTION

The tests in this section provide a means of fully testing the 371XXA VNA system for proper operation and signal stability. These tests are intended to be used as a periodic check of the operational functionality of the 371XXA.

The tests should be performed in their entirety at least once annually. Although there is no requirement to do so, the tests should generally be run in the sequence presented.

NOTE

The procedures presented in Chapter 4, Performance Verification, provide the means to test the *accuracy* of the tests performed by the 371XXA.

Please ensure you have read and fully understand the servicing concepts for the 371XXA presented in Chapter 1 prior to continuing with this chapter.

Operational Tests for the 371XXA consist of the following:

- Checking the Service Log
- Self Test
- Peripherals and Interface Testing
- Signal Path Tests (includes Checking the Service Log and Self Test.)

These tests are described in paragraphs 3-2 through 3-5, which start on the next page.

3-2 CHECKING THE SERVICE LOG

Checking the service log consists of viewing the entries written into the log.

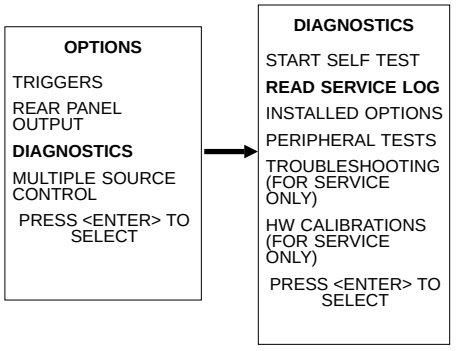
CAUTION

The service log contains historical information about instrument condition and any failures that may have occurred. It should be cleared only by a qualified service engineer. Such clearing should be accomplished only upon determining that the errors need not be saved to disk, or printed out for service purposes.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the OPTIONS menu (left); then select **READ SERVICE LOG** from the DIAGNOSTICS menu.



The 371XXA will now display the contents of the service log. The display consists of a header and an error listing. The header contains a variety of system service information. The error listing contains error messages for failures that may have occurred during operation.

NOTE

- Errors 7201–7209, GPIB remote operation programming errors, report that one or more external GPIB programming errors has been detected. These messages do not indicate a 371XXA system fault.
- Informational messages 0000–0099 report the pass/fail status of a peripheral access. These messages do not indicate a 371XXA system fault.

Any other error messages in the service log may indicate an instrument problem and should be investigated. Refer to the Chapter 5, Troubleshooting, for further information.

CAUTION

The **CLEAR SERVICE LOG** menu selection will immediately and permanently clear all the error message entries from the service log. (However, it will not clear the header information.) See Caution message at top of page.

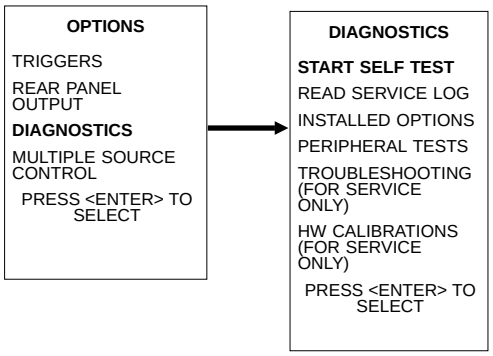
3-3 SELF TEST

The self test performs a series of tests that verify that various internal 371XXA circuits are functional and operating properly. Note that a semi-rigid cable must be connected between front panel connectors Source Lock Output and a1.

To start the self test:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** fromthe OPTIONS menu; then select **START SELF TEST** (below).



Step 3. Wait for test sequence to complete. (Once invoked, this test requires no user interaction or external equipment.)

Upon completion, the net pass/fail result of the self test is shown on the CRT display. If the 371XXA is in remote-only operation, the results are reported via the GPIB output buffer. If the self test fails, detailed error messages will be written into the service log.

If self test fails:

- ❑ Check the service log to view failure messages.
- ❑ Proceed to Chapter 5, Troubleshooting.

3-4 PERIPHERALS AND INTERFACES TESTS

These tests are used to verify the operation of the CRT display, front panel keys, and peripheral devices that are used with the 371XXA. They consist of the following:

- CRT Display Test
- Front Panel Test
- External Keyboard Interface Test
- Printer Interface Test
- GPIB Interface Test

CRT Display Test

This test verifies that the 371XXA CRT display is functioning correctly.

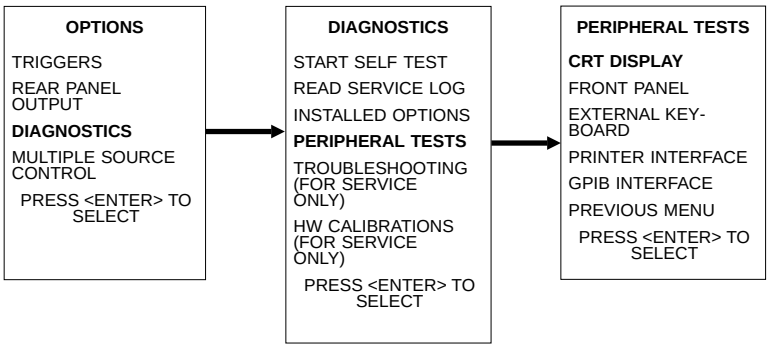
NOTE

The External VGA Out Connector can also be tested when using this procedure if an external VGA monitor is connected.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu; then in sequence select: **PERIPHERAL TESTS**, and then **CRT DISPLAY**. See diagram below.



Step 3. Follow instructions on the CRT screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

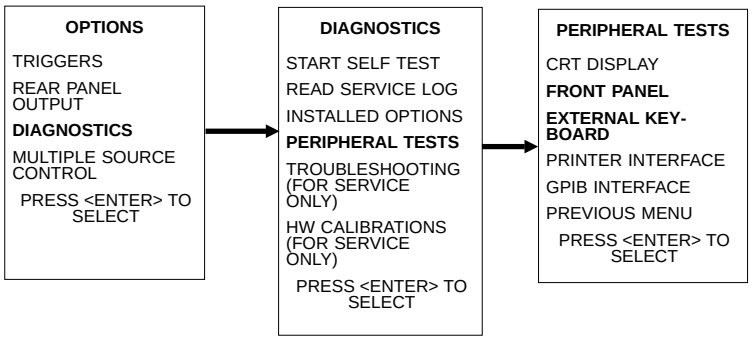
Front Panel Test

This test verifies that the control keys in each of the 371XXA key groups are functioning correctly.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** fromthe OPTIONS menu; then in sequence select: **PERIPHERAL TESTS**, and then **FRONT PANEL**. See diagram below.



Step 3. Follow instructions on the screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

External Keyboard Interface Test

This test verifies that the 371XXA external keyboard interface is functioning correctly.

Equipment Required:

An IBM compatible keyboard is required for this test.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** fromthe OPTIONS menu; then in sequence select: **PERIPHERAL TESTS**, and then **EXTERNAL KEYBOARD**. See diagram above.

Step 3. Follow instructions on the screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

Printer Interface Test

This test verifies that the 371XXA printer interface is functioning correctly.

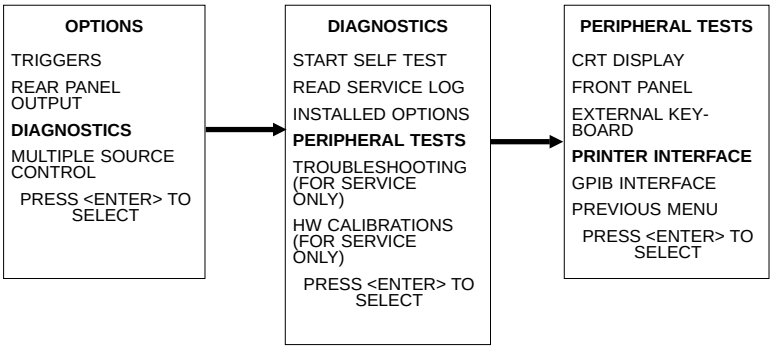
Equipment Required:

Printer Test Fixture (ANRITSU PN: B39553)

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu; then in sequence select: **PERIPHERAL TESTS**, and then **PRINTER INTERFACE**. See diagram below.



Step 3. Follow instructions on the screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

GPIB Interface Test

This test verifies that the 371XXA printer interface is functioning correctly.

Equipment Required:

GPIB cable (ANRITSU PN: 2100-2), or equivalent

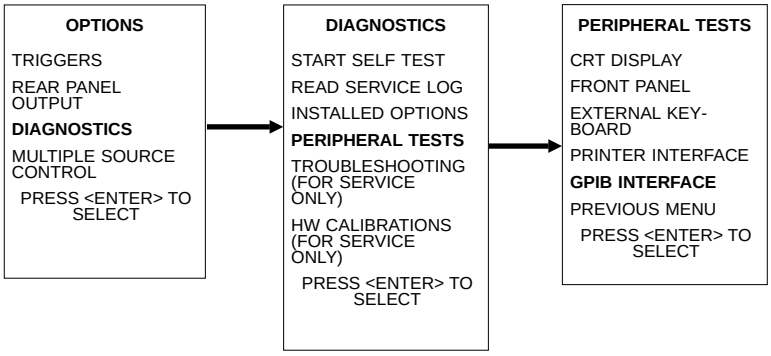
CAUTION

Insure that no other cables are connected to either of the two rear panel GPIB ports when performing this test.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu; then in sequence select: **PERIPHERAL TESTS**, and then **GPIB INTERFACE**. See diagram below.



Step 3. Follow instructions on the screen until test is completed.

If test fails, proceed to Chapter 5, Troubleshooting.

3-5 SIGNAL PATH TESTS

These are a series of automated tests designed to insure the 371XXA internal signal paths are functioning properly and are capable of supporting stable calibrations and measurements. These test are performed using a software test program and an external computer/controller.

The test software performs the following operations and tests:

- Service Log Check
- Self Test
- Basic Sweep Operation and Speed Test
- High Level Noise Test
- System Stability Test
- RF Power Generation and Control Test
- Sampler Efficiency and Stability Test
- LO1/LO2 Linearity Test
- Source FM/Lock Signal Linearity Test

Equipment required:

37XXX Test Software (ANRITSU PN: 2300-178)

IBM Compatible PC with VGA Graphics Adapter and Mouse

External computer/controller; refer to Table 1-1 located on page 1-8.

GPIB cable (ANRITSU PN: 2100-2), or equivalent

Procedure:

Step 1. Using the GPIB cable, connect the external computer/controller to the IEEE 488.2 GPIB Interface port on the 371XXA rear panel.

Step 2. Change to directory 3700DIAG, and type **`3700test`** at the DOS prompt. (Note: Program will not run from the floppy disk.)

NOTE

Install test software (ANRITSU PN: 2300-178) to the hard drive. (Insert software disk in floppy drive and — depending on whether 3.5-inch floppy is A: or B: — at the DOS prompt, type **`A:\INSTALLA or B:\INSTALLB.)`**

Step 3. After entering operator name and instrument information, select Individual Tests. Then select Transmission Tests.

Step 4. Follow the directions displayed on the computer screen to perform all tests.

If any tests fail, refer to the Troubleshooting and Help selections of the Test Software menu for assistance.

Chapter 4
Performance Verification

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Chapter 4
Performance Verification

4-1 INTRODUCTION

This chapter provides specific procedures to be used to verify that the 371XXA is making accurate, traceable S-parameter measurements. You should perform the verification procedures in paragraph 4-3, "Verifying Measurement Accuracy," at least once annually.

Additionally, this chapter includes procedures that may be used to measure the following key system performance parameters:

- Sampler Efficiency
- High Level Noise
- Compression Level
- Noise Floor/Receiver Dynamic Range
- Frequency Accuracy
- Power Level Accuracy

The Operational Tests described in Chapter 3 should be performed prior to verifying system performance.

Please ensure you have read and fully understand the servicing concepts for the 371XXA presented in Chapter 1 prior to continuing with this chapter.

4-2 CALIBRATION AND MEASUREMENT CONDITIONS

Extremes in the surrounding environmental conditions and the condition and stability of the test port connectors, through-cable, and calibration kit determine system measurement integrity to a large extent.

These are all user controlled conditions, and as such, should be evaluated periodically for impact on system performance. If these conditions vary significantly with time, the system verification procedures should be performed more often than the recommended annual cycle.

Standard Conditions

The standard conditions specified below must be observed when performing any of the operations in this chapter — both during calibration and during measurement.

Warm-up Time: One hour minimum.

Environmental Conditions:
Temperature: 23 +/- 3 deg C
Relative Humidity: 20– 50% recommended.

Special Precautions

When performing the procedures in this chapter, observe the following precautions:

- Minimize vibration and movement of system and attached components and through-cable.
- Clean and check pin depth and condition of all adapters, through-cable(s), and calibration components.
- Pre-shape the through-cable(s) so as to minimize its movement during calibration and measurement activities.
- Ensure the system remains motion free in stable environmental conditions as defined above throughout warm-up, calibration, and measurement activities.

4-3 PERFORMANCE VERIFICATION PROCEDURE

The following are the specific tests that should be used to verify the performance of the 371XXA. Equipment required for these tests is shown below.

Qty	Item
1	ANRITSU 3652-1 Calibration Kit
1	EIP 548 Frequency Counter
1	HP 437 Power Meter
1	HP 8487A Power Sensor
1	ANRITSU ND45331 Test Fixture Kit
1	ANRITSU ND45332 Test Fixture Kit
1	ANRITSU 3670K50-1 Through Cable
1	ANRITSU 3670K50-2 Through Cable
1	ANRITSU 41KC-10 with Option C
2	ANRITSU 43KC-3
1	ANRITSU 33KFKF50 Insertible

Equipment Required

Required equipment in listed above.

Sampler Efficiency Test

This test verifies that each individual receiver channel operates properly. Measurement calibration of the system is not required for this test. This test requires that you press specified front panel keys and make choices from the displayed menu(s).

Test Setup

Step 1. Connect Test Fixtures ND45331 and ND45332 to the 371XXA as shown in Figure 4-1 on the next page.

Step 2. Reset the 371XXA using the Default Program key.

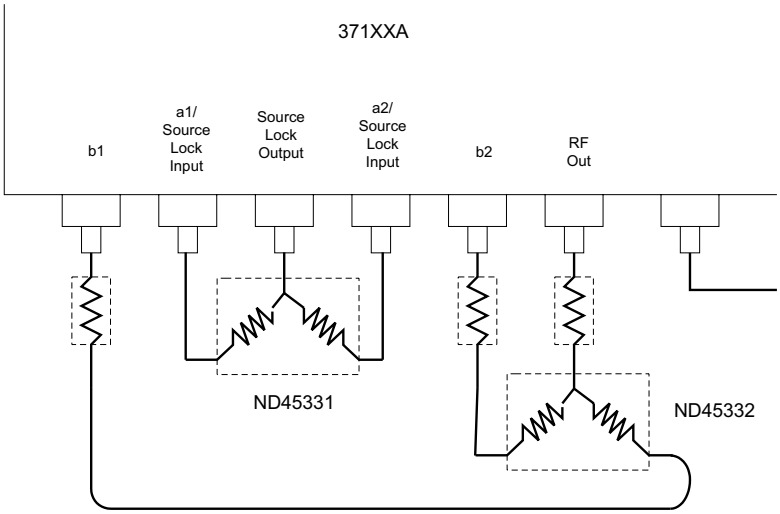


Figure 4-1. *Connecting the Test Fixtures*

Step 3. Set up the 371XXA as shown below.

Key	Menu Choice
Options Menu	Non-Ratioed Parameters
Setup Menu	START: 1 GHz STOP: High End Frequency
Channel Menu	Four Channels
Graph Type	Log Magnitude (All channels)

Test Procedure

Step 1. Observe sweep indicators and allow at least one complete sweep to occur on all four channels.

Step 2. Verify that the maximum-value to minimum-value amplitude slope meets the following specifications:

Model	High-End Frequency	Reference Channel Slope	Test Channel Slope
37147A	20 GHz	® 10 dB	® 12 dB
37169A	40 GHz	® 12 dB	® 14 dB

Step 3. Verify that the minimum amplitude meets the specifications shown below.

Model	Test Channel	Reference Channel
37147A	–26	–28
37169A	–38	–36

NOTE

Use the Marker Menu and Readout Marker keys and menus to obtain precise frequency and amplitude values.

Step 4. Press the Option Menu key, and select DIAGNOSTICS.

Step 5. Select TROUBLESHOOTING

Step 6. Select FINISHED, RECOVER FROM TROUBLESHOOTING.

NOTE

If Steps 4 through 6 are not performed, the system will be locked in the TROUBLESHOOTING state and cannot be used to perform normal measurements.

High Level Noise Test

The following test verifies that the high-level signal noise in the 371XXA will not significantly affect the accuracy of subsequent measurements. Calibration of the system is not required for this test. This test requires that you press specified front panel keys and make choices from the displayed menu(s).

Test Procedure

Step 1. Reset the 371XXA using the Default Program key.

Step 2. Set up the 371XXA as shown below.

Key	Menu Choice
Setup Menu	START: 40 MHz STOP: High-end Frequency
Channel Menu	DUAL CHANNEL 1-3
Graph Type	LOG MAGNITUDE (both channels)
Set Scale	RESOLUTION: 0.020 dB/Div REF VALUE: 0.0 dB (both channels)
S-Params	Channel 1 - S12 Channel 3 - S21
Data Points	201
Video IF BW	NORMAL (1 KHz)
Limits	UPPER LIMIT ON 0.015 dB 37147A or 0.040 dB 37169A LOWER LIMIT ON –0.015 dB 37147A or –0.040 dB 37169A DISPLAY LIMITS ON

Step 3. Connect the ND45331 and ND45332 test fixtures to the 371XXA (See Figure 4-1).

Step 4. Press the Ch 1 key.

Step 5. Press the Trace Memory key.

Step 6. Choose VIEW DATA from the menu and press the Enter key.

Step 7. While observing the sweep indicators, allow at least two complete sweeps to occur.

Step 8. Choose STORE DATA TO MEMORY from the menu and press the Enter key.

Step 9. Choose VIEW DATA (/) MEMORY from the menu and press the Enter key.

Step 10. While observing the sweep indicators, allow at least two complete sweeps to occur.

Step 11. Verify that the peak-to-peak High Level Noise falls within the area between the two limit lines (Figure 4-2).

Step 12. Press the Ch 3 key.

Step 13. Repeat steps 4 through 11 for channel 3.

Compression Level Test As RF power is increased, at some point the sampler will start to become non-linear. When the sampler detected value is 0.1 dB less than the RF input power level, the sampler is at the 0.1 dB compression point (below).

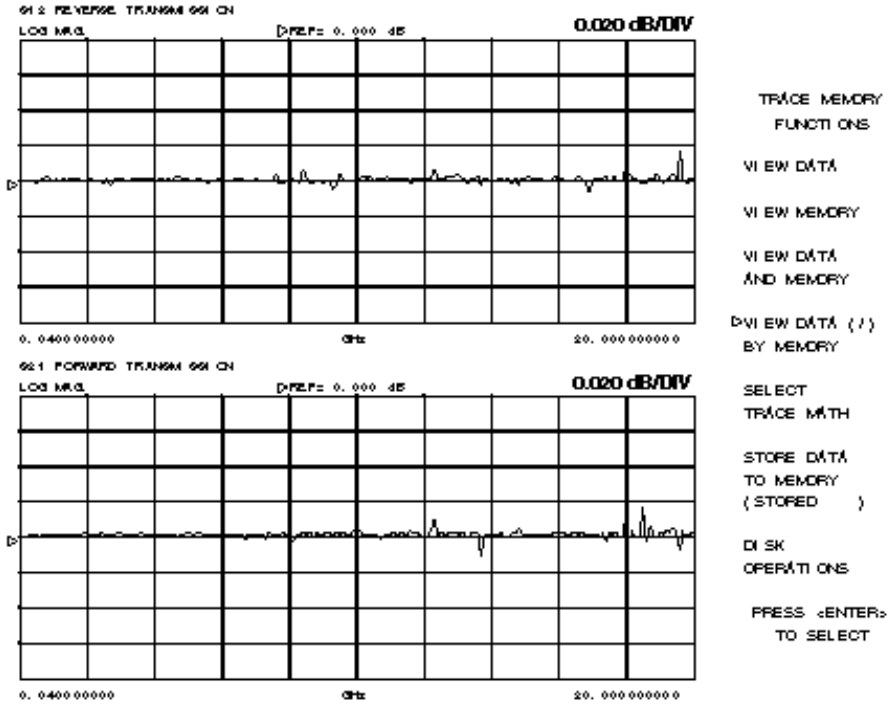


Figure 4-2. *High Level Noise Test Waveform*

Step 14. This test verifies that the compression level is 0.1 dB or less for a specified power input level (below).

Frequency (GHz)	Max. signal level for 0.1dB Compression(dBm)
0.5	–12
2	–12
20	–12
40	–15

b1 Channel Verification Procedure

Step 1. Set up the 371XXA as shown below.

Key	Menu Choice
SETUP MENU	DISCRETE FILL; Insert the following frequencies: 500 MHz, 2 GHz, 20 GHz, and 40 GHz if applicable
CHANNEL MENU	SINGLE CHANNEL
GRAPH TYPE	LOG MAGNITUDE
S-PARAMS	S11
SET SCALE	RESOLUTION: 20 dB/DIV, REF VALUE: 0 dB

Step 2. Set up the equipment as shown in Figure 4-3, below.

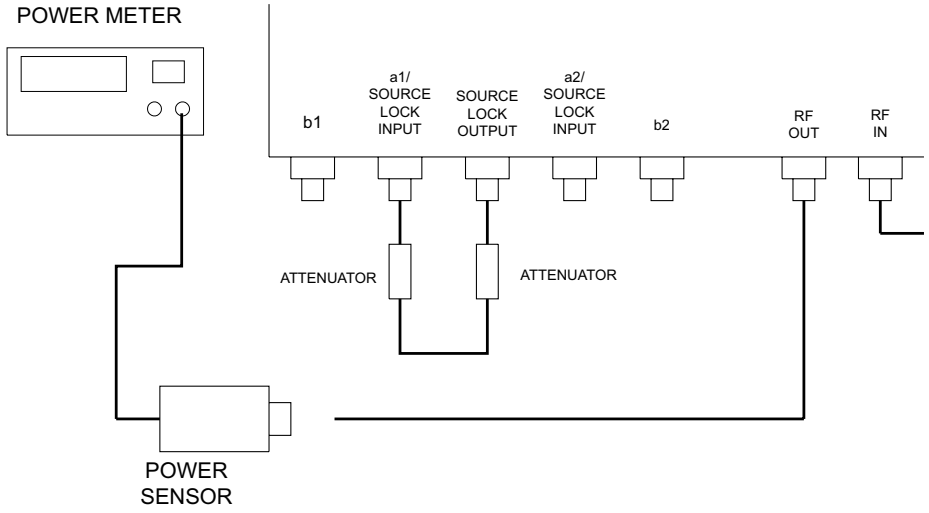


Figure 4-3. *b1 Channel Verification Setup*

Step 3. Zero and calibrate the Power Sensor and then connect the Power Sensor to the unterminated end of the cable connected to RF Out.

Step 4. Press the Setup Menu key.

Step 5. Select C.W. MODE and press the Enter key.

Step 6. Set the C.W. Frequency for the first frequency listed in Table 4-3 (500 MHz) if this is the first time through this step. Set the C.W. Frequency for 2 GHz for the second time through, 20 GHz for the third time, and so on.

Step 7. Select TEST SIGNALS.

Step 8. Move the cursor to POWER CONTROL when the next menu appears, and adjust the level for –12 dBm ∫0.1 dB as indicated on the Power Meter. Use an attenuator if necessary and set the appropriate Cal Factor on the Power Meter as required for each frequency.

NOTE

Adjust the POWER CONTROL level for –15 dBm ∫0.1 dB if the C.W. Frequency is set for 40 GHz in Step 6.

Step 9. Connect a 41KC-10 Attenuator to the unterminated end of the cable connected to RF Out.

Step 10. Connect the unterminated end of the 41KC-10 Attenuator to b1.

Step 11. Press the Trace Memory key.

Step 12. Select VIEW DATA and wait one complete sweep, then select STORE DATA TO MEMORY, VIEW DATA (/) MEMORY.

Step 13. Remove the 41KC-10 and re-connect the cable to b1.

Step 14. Set Marker 1 on, press the Readout Marker key and note the value.

Step 15. Find the attenuation value of the 41KC-10 at the corresponding frequency. Use the formula below to find the variation value between the two power levels.

[Variation value] = [Attenuation value of 41KC-10] - [Readout value]

The Variation value should be less than 0.1 dB.

Step 16. Repeat Steps 6 through 15 for 2 GHz, 20 GHz, and 40 GHz as applicable.

b2 Channel Verification Procedure

Step 1. Set up the 371XXA as shown below.

Key	Menu Choice
SETUP MENU	DISCRETE FILL; Insert the following frequencies: 500 MHz, 2 GHz, 20 GHz, and 40 GHz if applicable
CHANNEL MENU	SINGLE CHANNEL
GRAPH TYPE	LOG MAGNITUDE
S-PARAMS	S22
SET SCALE	RESOLUTION: 20 dB/DIV, REF VALUE: 0 dB

Step 2. Set up the equipment per Figure 4-4.

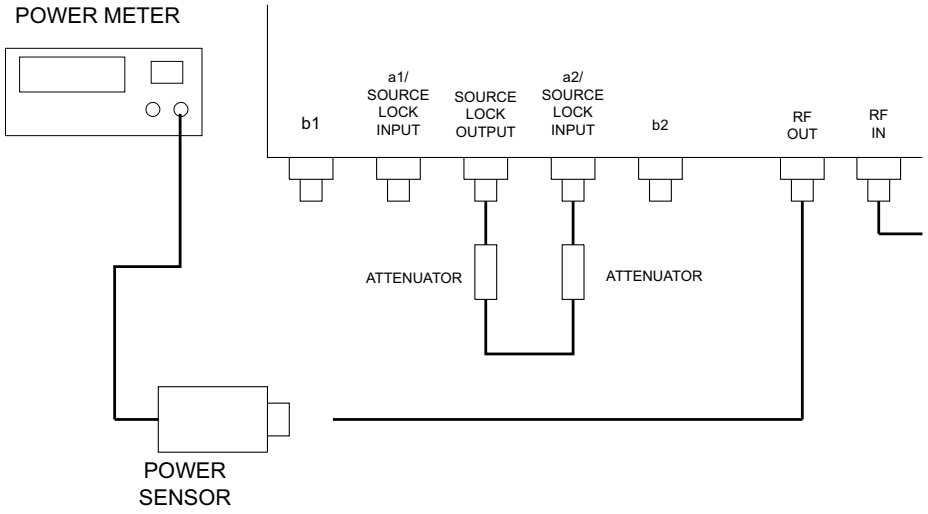


Figure 4-4. *b2 Channel Verification Setup*

Step 3. Zero and calibrate the Power Sensor and connect it to the unterminated end of the cable connected to RF Out.

Step 4. Press the Setup Menu key.

Step 5. Select C.W. MODE and press Enter.

Step 6. Set C.W. Frequency for the first frequency listed in Table 4-3 (500 MHz) if this is the first time through this step. Set the C.W. Frequency for 2 GHz for the second time through, 20 GHz for the third time, and so on.

Step 7. Select TEST SIGNALS.

Step 8. Move the cursor to POWER CONTROL when the next menu appears, and adjust the level for –12 dBm, ±0.1 dB as indicated on the Power Meter. Use the attenuator if necessary and set the appropriate Cal Factor on the Power Meter as required for each frequency.

NOTE

Adjust the level for –15 dBm, ±0.1 dB if the C.W. Frequency is set for 40 GHz in Step 6.

Step 9. Connect a 41KC-10 Attenuator to the unterminated end of the cable connected to RF Out.

Step 10. Connect the unterminated end of the 41KC-10 Attenuator to b2.

Step 11. Press the Trace Memory key.

Step 12. Select VIEW DATA and wait one complete sweep.

Step 13. Select STORE DATA TO MEMORY, then select VIEW DATA (/) MEMORY.

Step 14. Remove the the 41KC-10 and re-connect the cable to b2.

Step 15. Set Marker 1 on, press the Readout Marker key, and note the value.

Step 16. Find the attenuation value of the 41KC-10 at the corresponding frequency. Use the formula below to find the variation value between the two power levels.

[Variation value] = [Attenuation value of 41KC-10] - [Readout value]

Variation value should be less than 0.1 dB.

Step 17. Repeat Steps 6 through 15 for 2 GHz, 20 GHz, and 40 GHz as applicable.

Noise Floor/Receiver Dynamic Range Test

Noise Floor is the small signal response resulting from noise. It establishes the lowest level of signal detection. The Receiver Dynamic Range is the difference between the receiver compression level and the noise floor. This test verifies that the noise floor meets the guaranteed performance specifications.

Test Procedure Part A, Set Source Power Level

The following test uses a Power Meter to calibrate the Source output power setting at specified frequency points across the Frequency coverage range of the 371XXA.

Step 1. Set up the equipment per Figure 4-5. Do not connect the Power Sensor to RF Out at this time.

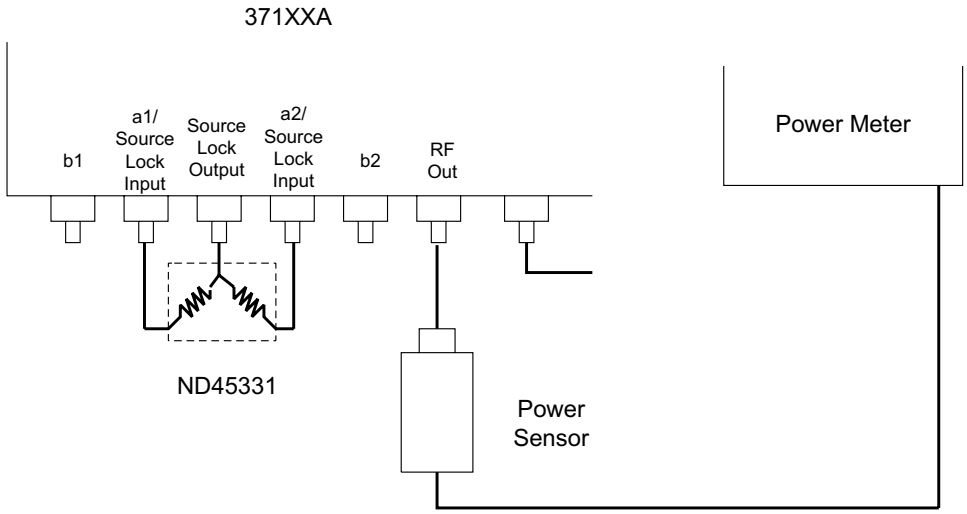


Figure 4-5. *Source Power Level Setup*

Step 2. Zero and calibrate the Power Sensor, then connect it to RF Out.

Step 3. Press the Setup Menu key and select TEST SIGNALS.

Step 4. Move the cursor to C.W. MODE and press the Enter key.

Step 5. Set C.W. Frequency for the first frequency listed below (22.5 MHz) if this is the first time through this step. Set C.W. Frequency for 2 GHz for the second time through, 20 GHz for the third time, and so on.

Frequency (GHz)	Power Control Setting
0.0225	
2	
20	
40	

Step 6. Move the cursor to POWER CONTROL when the next menu appears, and adjust the level for –12 dBm ±0.1 dB as indicated on Power Meter. Use the attenuator if necessary and set the appropriate Cal Factor on the Power Meter as required for each frequency. Note: Adjust the level for -15dBm ±0.1 dB if C.W. Frequency is set for 40 GHz in Step 5.

Step 7. Record the POWER CONTROL setting in Step 5, above.

Step 8. Repeat Steps 5 through 7 for the rest of the frequencies listed Step 5, above.

Test Procedure Part B, Noise Floor/Receiver Dynamic Range

The following test verifies the Receiver Dynamic Range and Noise Floor performance.

Step 1. Set up the equipment per Figure 4-6.

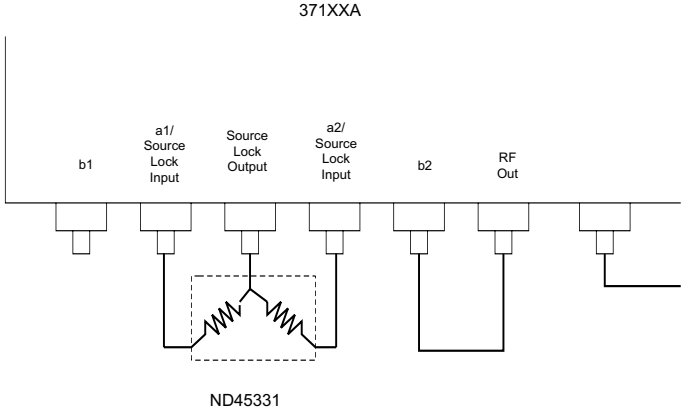


Figure 4-6. *Noise Floor/Receiver Dynamic Range Setup*

Step 2. Set the 371XXA as shown below.

Key	Menu Choice
CHANNEL MENU	SINGLE CHANNEL
S-PARAMS	S21 (Channel 1)

Step 3. Press the Begin Cal key.

Step 4. Select from the displayed prompts to perform a C.W. (1 POINT), STANDARD, COAXIAL, TRANSMISSION FREQUENCY RESPONSE (S21) Calibration for the first frequency listed in Table 4-6 (22.5 MHz) if this is the first time through this step. Set C.W. Frequency for 2GHz for the second time through, 20 GHz for the third time and so on. Note: When prompted for isolation devices, connect terminations to b2 and RF Out.

Step 5. When the CONFIRM CALIBRATION PARAMETERS menu appears, select TEST SIGNALS.

Step 6. Set the POWER CONTROL selection to the power level recorded in Table 4-6 for the applicable frequency, then select RESUME CAL.

Step 7. Follow the displayed prompts to complete the calibration.

Step 8. Disconnect the cable from b2 and RF Out and connect 50 ohm terminations to b2 and RF Out.

Step 9. Set up the 371XXA as shwo.

Key	Menu Choice
GRAPH TYPE	LOG MAGNITUDE
SET SCALE	RESOLUTION: 20 dB/DIV, REF VALUE: –80 dB
DATA POINT	POINT DRAWN IN C.W. 20
AVG/SMOOTH MENU	AVERAGING: 512 MEAS. PER POINT
AVERAGE	ON
VIDEO IF BW	MINIMUM

Step 10. Press the Trace Memory key.

Step 11. Select VIEW DATA and wait one complete sweep, then select STORE DATA TO MEMORY.

Step 12. Select VIEW DATA (-) MEMORY. Note: Use the SELECT TRACE MATH menu option to change to VIEW DATA (-) MEMORY.

Step 13. Allow one full sweep to occur, then press the Hold key.

Step 14. Press the Marker Menu key and enable MARKER 1.

Step 15. Press Readout Marker key, select MARKER TO MAX and record the value in the "Dynamic Range" column below.

Frequency (GHz)	Dynamic Range (dB)	Specification
0.0225		104
2		94
20		91
40		85

Step 16. Repeat Steps 3 through 15 for the rest of applicable frequencies listed in Step 15, above..

Step 17. Calculate the Noise Floor and record it below.

Frequency (GHz)	Noise Floor (dBm)	Specification
0.0225		–116
2		–106
20		–103
40		–100

Step 18. The formula is:

Noise Floor (dBm) =
Max. PWR Level for 0.1dB Compression – Dynamic Range (dB)

Example: For 22.5 MHz, max. PWR Level for 0.1 dB Compression is –12 dBm.

4-4 MEASUREMENT OF KEY SYSTEM PERFORMANCE PARAMETERS

The following paragraphs describe procedures for automated measurement of the key system performance parameters listed below. Measurement of these parameters is not required for system verification; however, it is highly recommended to ensure that the complete 371XXA measurement environment is stable and capable of supporting accurate measurements.

- Frequency Accuracy
- Power Level Accuracy

Measurement Environment Considerations

As with the verification procedures, the quality of the measurement of the system performance parameters listed above is very dependent on the measurement environment.

The complete 371XXA measurement environment consists of:

- Condition and stability of the test ports and through-cable mating connectors.
- Settings and stability of the surrounding environment, especially temperature, humidity, and vibration. To maintain the highest system performance, avoid changing these conditions, especially temperature, during warm-up, calibration, and when making measurements on the DUT.
- The use of proper microwave connector mating techniques.

Measurement Technique

The measurements of the key system performance parameters are performed using the ANRITSU 37XXX Test Software, PN: 2300-178.

NOTE

The Standard Conditions and Special Precautions should be observed when performing these measurements.

The software will use the following standards to determine system performance values:

- Frequency Counter
- Power Meter

Equipment Required

37XXX Test Software (ANRITSU PN: 2300-178)

IBM Compatable PC with VGA Graphics Adapter

External computer/controller; refer to Table 1-1 located on page 1-8.

GPIB cable (ANRITSU PN: 2100-2), or equivalent

Measurement Procedure

Step 1. Using the GPIB cable, connect the external computer/controller to the the 371XXA IEEE 488.2 GPIB rear panel connector.

Step 2. Change directory to 3700DIAG and type **`3700test`**.

NOTE

Install test software (ANRITSU PN: 2300-178) to the hard drive. (Insert software disk in floppy drive and — depending on whether your 3.5-inch floppy is A: or B: — at the DOS prompt, type **`A:\INSTALLA or B:\INSTALLB.`**)

Step 3. Follow the directions displayed on the computer screen to perform all tests.

If any tests fail, refer to the Troubleshooting and Help selections of the Test Software menu for assistance.

NOTE

To exit the program, click on the left-arrow icon to back out to the MAIN screen with OPERATOR INFORMATION window opened; then, simultaneously press keys ,<Ctrl + C> or <Ctrl + Break>.

Chapter 5
Troubleshooting

Table of Contents

Many of the troubleshooting procedures presented in this chapter require the removal of instrument covers to gain access to printed circuit assemblies and other major assemblies.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many assemblies in the 371XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

CAUTION

Never operate the 371XXA with connector J3 of the A21A2 Source Control PCB disconnected. Operation

Chapter 5
Troubleshooting

5-1 INTRODUCTION

This chapter provides specific procedures to be followed when troubleshooting 371XXA VNA systems. While performing these procedures, always observe the warnings and cautions on the opposite page.

To use the troubleshooting procedures in this chapter:

1. Select the paragraph heading (starting with paragraph 5-4) that best describes the nature of the 371XXA VNA system fault. Refer to the Table of Contents page.

2. Perform the procedure contained in the selected paragraph. In general, the steps within each procedure should be followed in the order presented.

3. When removing and replacing the various assemblies and components specified by the troubleshooting procedures in this chapter, refer to Chapter 8, Remove and Replace Procedures, as necessary.

4. If a step cannot be successfully completed, stop; correct the immediate problem, and then continue on to the next step until all the appropriate steps in the procedure are completed.

5. After troubleshooting and correcting a problem, perform the procedures in Chapter 3, (Operational Tests) and Chapter 4 (Performance Verification), as appropriate. This should be done to insure that the system has been fully and correctly restored to proper operation.

The procedures described in this chapter provide a general approach to troubleshooting 371XXA VNA problems. They are particularly useful for problems where the 371XXA is only partially functional. The Internal Diagnostic Menus described in Appendix A are very useful for evaluating 371XXA system performance. They may be used alone, or in conjunction with the procedures in this chapter.

Please ensure you have read and fully understand the servicing concepts for the 371XXA presented in Chapter 1 prior to continuing with this chapter.

Troubleshooting procedures for the millimeter wave feature, are provided in Appendix E.

5-2 ASSOCIATED INFORMATION IN THIS MANUAL

While using the troubleshooting procedures in this chapter, refer also the the following information:

- Appendix A, Diagnostics Menus, fully describes the 371XXA Diagnostics menu tree, including the SERVICE LOG menu.
- Appendix B, Error Codes and Messages, for details on each of the 371XXA hardware related error messages.
- Chapter 6, System Description, for a brief technical description of the 371XXA VNA system operation.

5-3 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for the troubleshooting procedures presented in this chapter is listed in Chapter 1, Table 1-1 (page 1-8).

5-4 IF SYSTEM DOES NOT POWER-UP

If the 371XXA does not power-up when connected to a source of AC power and the Power key is pressed, perform the power supply checks described below.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. TROUBLE-SHOOTING or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

Line Source and Interface Checks

Check as follows:

Step 1. Verify that the AC power source is providing stable power at the correct line voltage.

NOTE

The 371XXA is designed to automatically sense and operate with AC power line voltages in the range of 85 - 240 VAC, with a frequency of 48 - 63 Hz (540 VA maximum).

Step 2. Verify that the power input cord is in good condition.

Step 3. Ensure that the system power line fuse is installed, that it is not open, and that it is the correct value (8 A, Slow Blow).

Power Supply Voltages Check

Verify that the 371XXA power supply voltages are correct as follows:

Step 1. Press the 371XXA Power key **off**, and and disconnect the power input cord from the 371XXA. ensure all external connections to the system front and rear panel are also disconnected.

Step 2. Remove bottom panel, and lay the system down on its left (monitor) side. Refer to Chapter 8, Remove and Replace Procedures.

Step 3. Reconnect the power line input cord to the system and Press the 371XXA Power key **on**.

Step 4. Using a DMM or an oscilloscope, measure the DC power supply voltages listed in Table 5-1. Connect the DMM/oscilloscope to the top of the cable connectors at J13 and J4 on the Motherboard (A17). Refer to Figure 5-1 and Table 5-1.

Table 5-1. *371XXA DC Power Supply Voltage Checks*

Connect To:			DC Supply Voltage		AC Ripple and Noise
Conn	Com (Pin)	Meas (Pin)			
J13	8	16	0 Vdc		50 mVpp
J13	8	1	+4.8 Vdc	+1% / –0%	50 mVpp
J4	4	1	+9 Vdc	+5% / –0%	100 mVpp
J4	4	6	+18 Vdc	+10% / –0%	100 mVpp
J4	4	10	–18 Vdc	+10% / –0%	100 mVpp
J4	4	12	+27 Vdc	+5% / –0%	100 mVpp
J4	4	14	–27 Vdc	+5% / –0%	100 mVpp

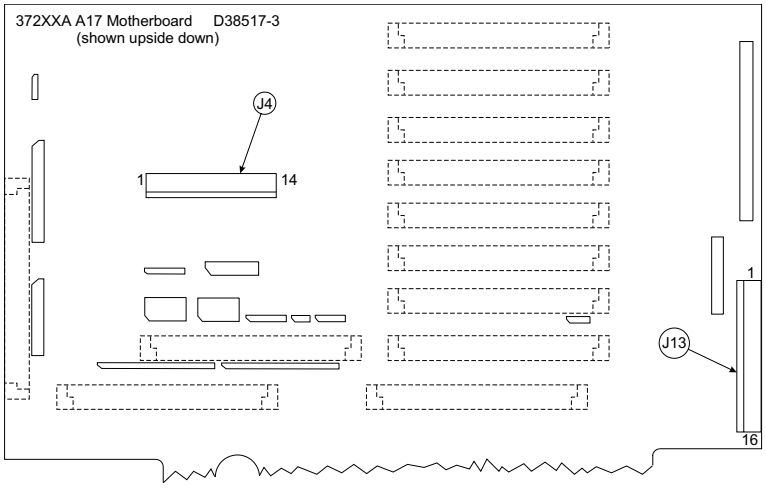


Figure 5-1. *Location of Connectors for Power Supply Voltage Checks*

Step 5. Connect the common lead of the oscilloscope to J13, pin 8. Measure the Power Supply Sync signal (PS_SYNC) on J13, pin 14:
Specification: 2-4 vpp Sine Wave at 109.89 KHz

NOTE

The power supply module will power-up without the PS_SYNC signal being present. However, the lack of this signal will introduce signal purity problems when the system is performing measurements.

Power Supply Module Check

If any of the DC voltage tests fail, verify that the power supply module is operating properly with minimal impact from the system as described in the procedures below.

NOTE

If a power supply voltage is low, it may be due to excessive current draw from the system and not a fault in the power supply.

Steps 1 through 4 verify the operation of the + 9,± 18, and ± 27 Vdc supplies:

Step 1. Press the 371XXA Power key **off**, and and disconnect the power input cord.

Step 2. Disconnect the power supply module from the A17 Motherboard at J4.

Step 3. Reconnect the power line input cord to the system and press the 371XXA Power key **on**.

Step 4. Using a DMM and/or an oscilloscope, measure the power supply voltages at the power supply connector pins that correspond to the Motherboard pins for the + 9, ± 18, and ± 27 Vdc supplies. Refer to Table 5-1 and Figure 5-1 (previous page).

Steps 5 through 8 check the +5 volt supply. This power supply requires at least a 10% load to turn on. Therefore, at least one of the digital PCBs A9, A13, or A14 (which use the 5 volt supply) must be installed in the system during this procedure.

Step 5. Press the 371XXA Power key **off**, and reconnect the power supply module to the Motherboard at J4.

Step 6. Unplug digital PCB's A13 and A14.

Step 7. Press the 371XXA Power key **on**.

Step 8. Using a DMM and/or an oscilloscope, measure the +5 volt power supply at connector J13 on the Motherboard. Refer to Figure 5-1 and Table 5-1.

Step 9. Press the 371XXA Power key **off**, and and reinstall the A13 and A14 PCB's removed in Step 6.

If any of the DC voltage tests fail in steps 1 through 8 above, replace the power supply module.

If any of the DC voltage tests fail with the power supply module connected to the 371XXA Motherboard — but pass with it disconnected — then the most probable cause of the failure is that one of the 371XXA assemblies is demanding an excessive amount of current. To locate the failed assembly:

1. Press the 371XXA Power key **off**, and unplug a single assembly.

2. Press the 371XXA Power key **on**, and note if the failed power supply functions normally.

3. Repeat Steps 1 and 2 until an assembly is found that clears the power supply failure. The removed assembly is suspect and should be replaced.

5-5 IF SYSTEM DOES NOT BOOT-UP

If the 371XXA does not boot-up when it is powered-up, perform the checks described below.

Boot-up Process Sequence

The boot-up process is controlled by the firmware located on the A9 PCB assembly (processor PROM) The boot-up activities include:

- Testing and initializing the A9 Main Processor PCB
- Testing communication between the A9 PCB and the digital PCB assemblies (A13, A14, A15, A16). The following messages will be displayed at this juncture:
  - Initializing front panel knob (A14/A20)....
  - Initializing GPIB (A13/A18)....
  - Initializing external keyboard (A13)....
  - Initializing external trigger (A13/A5)....
  - Initializing front panel (A14/A20)....
- Loading of system software from disk into memory
- Starting operation of the system software.
- System is booting—message is displayed.

At this point, the system software continues the boot-up process by performing the following activities:

- Issues command to A15 PCB to change display from TEXT mode to GRAPHIC mode and display ANRITSU logo.
- Performs basic communication tests between the digital system (A13, etc.) and the analog subsystem (A1-A8, A21A1, A21A2); this is part of a minimal self test.

- Conducts an IF Calibration
- Resets and loads the front panel state that was in effect prior to the last power down
- Starts the measurement process

NOTE

The system software fully controls the 371XXA VNA system after boot-up (with operator intervention and guidance). The system software is only loaded once upon initial power up.

Troubleshooting Boot-up Problems

To start the troubleshooting of boot-up related problems, perform the following preliminary checks:

1. Note any error messages displayed on the CRT display during the boot-up process.
2. Observe the front panel and the display during the boot-up process for information as to which part of the process failed or did not execute.
3. Verify that the system power supplies are working properly as per paragraph 5-4, above. Note particularly the operation of power supplies immediately after power-up.
4. Try to boot the instrument from the floppy disk and repeat steps 1 and 2 above.

Upon completion of the preliminary checks (above), perform the following procedures, as appropriate.

Hard Disk Problem 1

If a hard disk problem is indicated during bootup from a floppy disk, but the system can bootup correctly from the hard disk:

Step 1. Boot up from the hard disk, then format the hard disk using the procedure below.

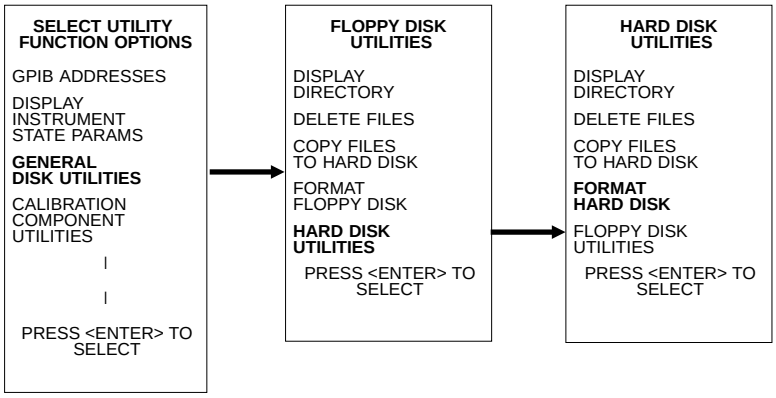
CAUTION

Formatting the hard disk will erase all files on the hard disk. Before starting the disk formatting process, copy any files you wish to save to a floppy disk.

Step 2. Press the Utility Menu key (System State key group) to display the **UTILITY FUNCTIONS OPTIONS** menu. From menu, select **GENERAL DISK UTILITIES** (see below).

Step 3. If **FLOPPY DISK UTILITIES** menu appears, select **HARD DISK UTILITIES**.

Step 4. From **HARD DISK UTILITIES** menu, select **FORMAT HARD DISK**.



Step 5. After formatting is complete, reload System Software from the master floppy diskettes. Retry boot-up. If fail, contact ANRITSU Customer Service Center.

Hard Disk Problem 2 If system does not bootup from hard disk and floppy disk:

Step 1. When the five initializing messages are displayed after power on, press any key within two seconds. Follow the on screen instructions to format the hard disk and re-load the System Software from the Master diskettes. If bootup still fails, go to the next step.

Step 2. Replace the A16 Hard Disk PCB.

Step 3. If bootup still fails, contact the nearest ANRITSU Customer Service Center.

Floppy Disk Problems If a floppy disk problem is indicated during bootup from floppy disk but the system is able to bootup from the hard disk:

Step 1. Ensure the floppy disk media is in good condition

Step 2. Verify disk drive connection at Motherboard connector J2.

Step 3. Retry boot-up. If fail, replace the A13 - I/O#1 PCB.

Step 4. Retry boot-up. If fail, replace the Floppy Disk Drive.

Screen Display Problems If the 371XXA system appears to have no screen display, perform the preliminary check below and then perform checks 1 - 3, as appropriate:

Preliminary Check - Press the 371XXA Power key **off** and then **on** several times. Each time power is reapplied, pause and wait for the

371XXA software system to boot-up. During boot-up, observe the top left hand portion of the CRT display.

NOTE

- An alternative method to reset and re-boot the software system is to press the red button on the A9 Main Processor PCB. Observe the messages displayed on the screen during the boot-up process. Verify that the following messages are present :
  - Initializing front panel knob (A14/A20)....
  - Initializing GPIB (A13/A18)....
  - Initializing external keyboard (A13)....
  - Initializing external trigger (A13/A5)....

Check 1: If during boot-up the 371XXA does not attempt to display any messages at all, proceed as follows:

Step 1. Replace the A15 Graphics Processor PCB.

Step 2. Retry boot-up. If fail, replace the Internal VGA Monitor.

Step 3. Retry boot-up. If fail, replace the A9, Main Processor PCB.

Step 4. Retry boot-up. If fail, contact ANRITSU Customer Service Center.

Check 2: If the system halts before it completes all five digital sections, process as follows:

Step 1. Replace the PCB indicated on the last displayed message. Example: If the system halt at the "Initializing front panel knob (A14/A20)....," replace the A14 and A20 PCBs.

Step 2. Retry to boot the system. If it still fails, contact ANRITSU Customer Service.

5-6 IF SYSTEM PRODUCES AN ERROR CODE

If the 371XXA detects a problem during normal operation, an error message consisting of an error code followed by a brief error message will be displayed on the screen. The error code will also be written to the service log along with some of the operating data gathered from the system at the time of failure. Note that as a reference signal must be applied to either the A1 or A2 input for the system to source lock, it is normal for error codes to be generated whenever a reference signal is not applied to A1 or A2. Install the ND45331 to prevent these phase lock error codes.

System error codes in the range 0100 - 3999 identify the suspected failed subassembly in the two most-significant digits of the error code. For example: error codes 0200 - 0299 are related to the A2, LO2 PCB assembly. This error code assignment scheme allows for quick identification of suspect assemblies.

NOTE

Refer to Appendix B, Error Codes/Messages, for a list of the error codes/messages for 37100A VNA systems.

There are cases when a fault on one assembly will cause a different assembly to be identified as faulty (per the error code designated). This happens when a failure occurs on an assembly that provides a stimulus or a calibration signal to other assemblies in the system. Example: the A7 LO3 PCB provides the IF Calibration signal to the A3, A4, and A6 PCB's. If the IF Cal signal is faulty, error codes will be reported for the A3, A4, A6, and A7 PCB's.

NOTE

An aide to troubleshooting system failures using error codes is a good understanding of system and subassembly operation. Refer to the descriptions of system and subassembly operation and block diagrams located in Chapter 7, System Description.

Self Test Error Codes

Error codes 0100 - 3999, with few exceptions, are produced as a result of a failure when the system self test is run. These error codes will **not** be displayed on the CRT screen. Only the overall result of the self test (PASS/FAIL) will be displayed at the conclusion of the self test. However, any error codes due to the self test will be written to the service log as the self test is executed.

NOTE

The exceptions are error codes with 00 in the two least-significant digits, for example: 0500 A/D CONVERSION FAIL. These errors are produced at run time if a problem is encountered when the system is actively making measurements.

Phase Lock Error Codes (6000 Series)

The Phase Lock error codes (6000 - 6999) will have an alphabetical suffix (code) following the message. For example: 6079 PHS LCK FAIL ABCDG. This code consists of one or more letters from A - G that represent the sub assembly that was not locked and/or the nature of the failure. The phase lock failure mode suffixes are listed below..

Failure Suffix	Failed Assembly/ Failure Mode	Failure Suffix	Failed Assembly/ Failure Mode
A	10 MHz not present	E	IF lock signal level too low
B	L01 unlocked	F	Ext synthesizer unlocked
C	L02 unlocked	G	L03 unlocked
D	Source unlocked	none	Unknown

Note that most phase lock error codes will normally consist of a letter identifying the unlocked assembly and the **D** and/or **DE** letters that indicate the Source Module is also unlocked. This is normal since all components in the phase lock loop must be correctly locked in order for the Source Module to achieve lock. Example 1: Any of the following error messages indicate that the LO1 PCB assembly was not able to lock:

```
6002 PHS LCK FAIL B
6010 PHS LCK FAIL BD
6026 PHS LCK FAIL BDE
```

Also note that if the 10 MHz Reference fails, depending on the failure, the system will not be able to lock any of the phase lock loop components: A1, A2, A7, A8, or Source Module. Example 2: Either of the following error messages indicate a 10 MHz Reference problem:

```
6001 PHS LCK A
6015 PHS LCK ABCDG
```

Service Log Snap Shot Data

Error codes will be written to the service log along with some data representing a "Snap Shot" of system conditions at the time of failure. Usually, the data included in the snap shot helps to provide faster diagnosis of the error condition. The common snap shot data items that will be useful in assembly level troubleshooting and fault diagnosis efforts are listed in Table 5-3.

Item	Description
SWP	Sweep direction: F = forward (S11, S21), R = reverse (S22, S12)
PWR	System source power setting
SYS	System frequency setting
A	The calibration results for the Test A Channel PCB (A3): This is a series of 16 values divided into groups of four. Each group should have values that are approximately ¼ that of those in the previous group. The first group data values should be approximately: 1.00 0.00 0.00 1.00. The values of the next group should be ¼ that of those values i.e., 0.25 0.00 0.00 0.25. The same applies for the values in the remaining two groups.
B	The calibration results for the Test B Channel PCB (A6). See description for "A" above.
R	The calibration results for the Reference A (or B) Channel PCB (A4). See description for "A" above.
<OVL>	Indicates the value was too far out of range to be measurable.
PHSLCK	Source Locking mode: L = Source Lock mode, T = Tracking mode, S = Set on mode

NOTE

Some of the data included in the snap shot is useful only for factory troubleshooting activities.

5-7 SIGNAL SOURCE, TEST SET, AND RECEIVER PROBLEMS

Because of the 371XXA phase-lock loop structure, it is not easy to distinguish between failures that occur in the Source Module, the Test Set Module and the Receiver Module. In order to troubleshoot failures occurring in this group of modules, it is essential to be familiar with how each module functions and how it interacts with the other modules. Refer to Chapter 7, System description, for a functional description of each module.

Signal Source Phase Lock Loop Assemblies

The 371XXA assemblies that contain circuits that are part of the signal source phase-lock loop (Source Lock function) are listed in Table 5-4.

Assemblies	Location
A21A1 Source YIG/Bias PCB	Source Module
A21A2 Source Control	Source Module
YIG Oscillator	Source Module
Switched Filter	Source Module
Down Converter	Source Module
Switched Doubler Module SDM*	Test Set Module
Power Splitter	Test Set Module
Buffer Amplifier	Receiver Module
A1 LO1 PCB	Receiver Module
A2 LO2 PCB	Receiver Module
A4 Reference IF PCB	IF Section
A8 Source Lock/Signal Separation Control PCB	Analog Subsystem
A9 Main Processor PCB	Digital Subsystem
* Model 37169A only	

Failures occurring in the Source Module, Test Set Module and Receiver Module will generally cause the system to produce “Phase Lock Fail” error codes. Included with the Phase Lock Fail error codes are alphabetical suffixes that indicate the probable malfunctioned sub-assembly.

Example: **6008 PHS LCK FAIL D**

The letter “D” in the error code above indicates that the failure is possibly in the Source Module. (Refer to Table 5-2.)

Signal Source/Test Set Module Error Codes

Failures occurring in the Signal Source Module and Test Set Module will also produce the error code listed in Table 5-5.

Error Code	Possible Failed Assemblies
5110 RF PWR UNLEVELED	All components in Source Module and Test Set Module

NOTES

If the 5110 error code is displayed when the Port 1 power level is set above the default power level, it does not indicate a failure. In this case, the 5110 error code is similar to the RF unleveled indicator on the Synthesizer or Sweep Generator.

The 371XXA has extensive built-in troubleshooting tools that are useful for troubleshooting the failure listed in Table 5-5. These and other troubleshooting tools are accessed from the Option Menu key, which is part of the enhancement keygroup. (From the select OPTIONS menu select **DIAGNOSTICS**, then select **TROUBLESHOOTING**). Refer to Appendix A.

Troubleshooting tools that are available from the TROUBLE-SHOOTING menu that are useful for locating faults occurring in the Source Module, Test Set Module and Receiver Module are:

NOTE

The troubleshooting tools listed below are used to test the 371XXA to factory set limits when the ANRITSU 37100A Test Software (2300-178) is run.

When run from the TROUBLESHOOTING menu, not all tests will display limit lines (as is the case when the 37100A Test Software 2300-178 is used).

NON-RATIO PARAMETERS

This function displays the output of each of the individual test set channels. It is especially useful for verifying the performance of the Buffer Amplifier and Power Amplifier.

NOTE

Installation of Test Fixtures ND45331 and ND45332 to the 37100A is required for this check.

By examining these displays in conjunction with other failure symptoms, the failed assembly can be located.

Example: Suppose the Non-Ratio Parameter screen display shows power holes above 270 MHz on all traces and in both sweep directions.

A possible cause for this condition is a failure of the Power Amplifier assembly at certain frequencies. (Refer to Analog Subsystem Block Diagram in Figure 7-2 on page 7-6).

LO1

This function allows user to verify whether the A1 LO1 PCB is operating properly.

LO2

This function allows the user to verify whether the A2 LO2 PCB is operating properly.

SOURCE

This function allows the user to verify whether the Source Module is operating properly.

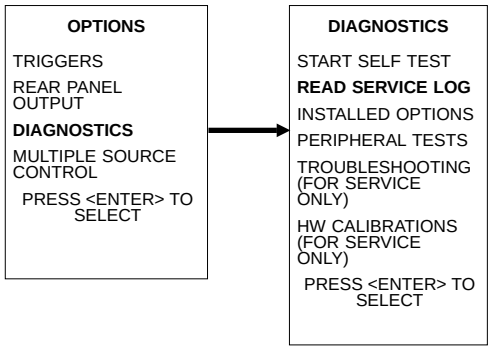
Isolation Procedures

The procedures in the following paragraphs will help you isolate the fault to the major assembly.

Check #1

Proceed as follows:

Step 1. Press Option Menu key and select the DIAGNOSTICS menu option.



Step 2. Select the READ SERVICE LOG menu option to display the error entry associated with the system failure. Observe the snap shot data included as part of the error entry and note the sweep direction indication for each error code. (Refer to Service Log Snapshot Data, page 5-11)

Step 3. Determine whether the failure occurs during forward measurements (S11, S21) and/or reverse measurements (S22, S12):

- If the problem occurs in both directions at all frequencies, the fault could be in the Receiver Module, Signal Source Module, or Test Set Module.

- If the problem occurs in both directions at only certain frequencies, the fault could be in the Signal Source Module.

- If the problem occurs in only one direction, the fault could be in the TEST SET MODULE.

Step 4. Run the 37XXX Test Software (2300-178) program to verify operation of the Buffer Amplifier, A1 LO1 PCB, A2 LO2 PCB, and Source control PCB.

Use the information obtained in steps 1 – 4 above to determine whether the failure occurs in the Source Module, Test Module or Receiver Module. Replace the suspected failed assembly, and perform any required adjustment(s). Then retest. If the 371XXA still fails, contact ANRITSU Customer Service Center for further assistance.

NOTE

To obtain technical service support from your nearest ANRITSU Customer Service Center, refer to Paragraph 1-9, Service Support Information.

Check #2 If you have determined that the failure occurs in both sweep directions, *only at certain frequencies*, and that Error Code 5110 is recorded in the Service Log, use the following procedures to determine which assembly may have failed:

Step 1. Set the 371XXA Start and Stop frequencies for the following bands:

Band	Start	Stop
1	22.5/40 MHz	2.0 GHz
2	2.0 GHz	Upper band-edge frequency for model. (20 GHz for 37169A)
3	20.0 GHz	40.0 GHz (for Model 37169A only)

Step 2. If the problem occurs in Band 1, replace the Down Converter assembly and repeat test.

If fail, contact ANRITSU Customer Service Center.

Step 3. If the problem only occurs in Band 3, replace the Switched Doubler Module assembly and repeat test.

If it fails, replace Switched filter and repeat test.

If it fails, contact ANRITSU Customer Service Center.

Step 4. If the problem only occurs in Band 2, replace Switched Filter assembly and repeat test.

If it fails, contact ANRITSU Customer Service Center.

NOTE

After replacing a component, perform a Frequency Calibration and a RF power/ALC Calibration. Refer to Chapter 6, Adjustments.

Check #3 If you have determined that failure occurs in both sweep directions, *at all frequencies* and Error Code 5110 is recorded in the Service Log, the failed component could be any of the following assemblies:

1. Switched Doubler Module
2. YIG Oscillator
3. A21A1 YIG Bias PCB
4. A21A2 Source Control PCB

Replace the components listed above in sequence. After each replacement recalibrate the unit (see note above) and retest. If the 371XXA still fails, contact your nearest ANRITSU Customer Service Center.

5-8 IF A PERIPHERALS/ INTERFACE TEST FAILED

The following paragraphs contain procedures to be used for troubleshooting 371XXA peripheral or interface test failures. Select the paragraph subheading that corresponds to the test that failed.

CRT Display Test Failures: If the CRT Display Test failed, troubleshoot as follows:

Step 1. Replace the CRT Monitor Assembly or LCD display.

Step 2. Perform the CRT Monitor Test again; if fail, replace the A15, Graphics Processor PCB.

Step 3. Perform the CRT Monitor Test again; if it fails, contact ANRITSU Customer Service Center.

Front Panel Test Failures: If the Front Panel Test failed, troubleshoot as follows:

Step 1. Replace the Front Panel Assembly.

Step 2. Perform the Front Panel Test again; if it fails, replace the A14, I/O#1 PCB.

Step 3. Perform the Front Panel Test again; if it fails, contact ANRITSU Customer Service Center.

External Keyboard Interface Test Failures: If the External Keyboard Interface Test failed, troubleshoot as follows:

Step 1. Replace the A18, Rear Panel PCB.

Step 2. Perform the External Keyboard Interface Test again; if it fails, replace the A13, I/O#1 PCB.

Step 3. Perform the External Keyboard Interface Test again; if it fails, contact ANRITSU Customer Service Center.

Printer Interface Test Failures: If the Printer Interface Test failed, troubleshoot as follows:

Step 1. Replace the A18, Rear Panel PCB.

Step 2. Perform the Printer Interface Test again; if it fails, replace the A13, I/O#1 PCB.

Step 3. Perform the Printer Interface Test again; if it fails, contact ANRITSU Customer Service Center.

GPIB Interface Test Failures: If the GPIB Interface Test failed, troubleshoot as follows:

Step 1. Replace the A18, Rear Panel PCB.

Step 2. Perform the GPIB Interface Test again; if it fails, replace the A13, I/O#1 PCB.

Step 3. Perform the GPIB Interface Test again; if it fails, contact ANRITSU Customer Service Center.

5-9 IF MEASUREMENTS ARE IN QUESTION

If the 371XXA measurement quality is suspect, the following paragraphs provide guidelines and hints for determining possible measurement quality problems.

The quality of 371XXA VNA measurements is determined by the following test conditions and variables:

- Condition of the 371XXA.
- Quality and condition of the interface connections and connectors.
- Quality and condition of the calibration components, through-lines, adapters and fixtures.
- Surrounding environmental conditions at the time of the measurement.

- Selection and performance of the calibration for the DUT being measured.

Measurement Conditions Check List

When determining possible measurement problems, check the following items:

1. Check the DUT and the calibration conditions:
   - Ensure the Calibration Components Coefficients data has been installed into the system from the Calibration Kit in use.
   - Ensure the proper calibration was done for the device being measured:
     - For high insertion loss device measurements the calibration should include isolation, high number of averages, and lower IF Bandwidth settings during the calibration.
     - For high return loss device measurements the calibration should also include a sliding load calibration.
   - Check DUT mating connector(s) condition and pin depth.
   - Measure an alternate known good DUT, if possible.
   - Check if the environment is stable enough for the accuracy required for the DUT measurement.
     - The system should not be subjected to variations in temperature.
     - The system should not be placed in direct sun light or next to a changing cooling source, such as a fan or air conditioning unit.
2. Check the calibration using known good components from the calibration kit. If measurements of these devices do not produce good results:
   - Check through-cable stability including condition and pin depth. Replace with a known good cable, if necessary.
   - Check condition and pin depth of calibration kit components. Replace with known good components, if necessary.
   - Check condition and pin depth of test port connectors. Replace with known good ones if necessary.

   NOTE

   The procedures for performing pin depth measurements for the connectors used on ANRITSU products are contained in Appendix C, Connector Maintenance Check Procedures.
3. Check the system performance as follows:

- Perform the Signal Path Tests that are part of the Operational Tests. Refer to Chapter 3, Operational Tests.
- Check Compression Level and Dynamic Range as described in Chapter 4, Performance Verification.
- Complete the remaining checks described in Chapter 4, Performance Verification.

Chapter 6
Adjustments

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Chapter 6
Adjustments

6-1 INTRODUCTION

This chapter contains four procedures that are used to restore the calibration of the 371XXA signal source and the related source lock system assemblies. Use these procedures after various signal source related assemblies have been replaced due to troubleshooting or repair activities.

Please insure you have read and fully understand the servicing concepts for the 371XXA presented in Chapter 1 prior to continuing with this chapter.

6-2 LO1 CALIBRATION

This procedure uses the 371XXA internal diagnostics and calibration menus to adjust the A1 1st LO PCB assembly. Perform this calibation procedure if:

- The A1 PCB is replaced.
- BBRAM chip on A9 Processor PCB is replaced and the LO1 Calibration data was not previously saved on disk (that is, data is not available for recall from a floppy disk).

Calibration Procedure

Perform the following steps:

Equipment Required

None

NOTE

Allow the 371XXA to warm-up at least 30 minutes prior to performing calibration.

Procedure

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS** then **LO1 CALIBRATION.**

Step 3. Follow the directions displayed on the 371XXA CRT screen, until calibration is completed.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS |DISK OPERATIONS |SAVE TO HARD DISK|HW_CAL.LO1.**

NOTE

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type, date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

If calibration fails:

Step 3. Repeat the calibration. If it still fails, then proceed to Chapter 5, Troubleshooting.

6-3 LO 2 CALIBRATION

This procedure uses the 371XXA internal diagnostics and calibration menus to adjust the A2 2nd LO PCB assembly. Perform this calibration procedure if:

- The A2 PCB is replaced.
- BBRAM chip on A9 Processor PCB is replaced and the LO2 Calibration data was not previously saved on disk (that is, data is not available for recall from a floppy disk).

Calibration Procedure

Perform the following steps:

Equipment Required

None

NOTE

Allow the 371XXA to warm-up at least 30 minutes prior to performing calibration.

Procedure

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS** then **LO2 CALIBRATION.**

Step 3. Follow the directions displayed on the 371XXA CRT screen, until calibration is completed.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS |DISK OPERATIONS |SAVE TO HARD DISK|HW_CAL.LO2.**

NOTE

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type (ALC), date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

If calibration fails:

Step 3. Repeat the calibration. If it still fails, then proceed to Chapter 5, Troubleshooting.

6-4 FREQUENCY CALIBRATION

This procedure uses the internal 371XXA diagnostics and calibration menus, in conjunction with a suitable frequency counter, to adjust the signal source frequencies throughout the range of the 371XXA model being calibrated. Perform this calibration procedure if:

- The Source FM/Lock Linearity test in Chapter 3, Operational Test, fails.
- Other testing or troubleshooting reveals a possible problem with the signal source frequency accuracy or phase lock loop.
- Any of the following assemblies are replaced:
  - A21A1 Source YIG/Bias
  - A21A2 Source Controller

- Down Converter
- YIG Oscillator
- Switched Filter

- ❑ BBRAM chip on the A9 Processor PCB is replaced and the Source Calibration Data was not previously saved on disk (thus data could not be recalled from disk).

Calibration Procedure

Perform the following steps:

Equipment Required

Refer to Table 1-1, located on page 1-8, for further information about the following equipment:

EIP Model 578B Frequency Counter, or equivalent.

RF/Microwave Cable

GPIB cable, ANRITSU 2100-2, or equivalent

NOTE

Allow the 371XXA and Frequency Counter to warm-up for at least 30 minutes prior to performing calibration. If testing a 37147A, add a 6 or 10 dB pad to counter input.

Procedure

Step 1. Connect test equipment as shown in Figure 6-1.

Step 2. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 3. Select **DIAGNOSTICS** from menu; then select in sequence: **H/W CALIBRATION**, and then **SOURCE FREQUENCY CALIBRATION** (next page).

Step 4. Follow the directions displayed on the screen to set-up and connect the frequency counter to the 371XXA.

Step 5. Select **START SOURCE FREQ CALIBRATION** from the menu (above).

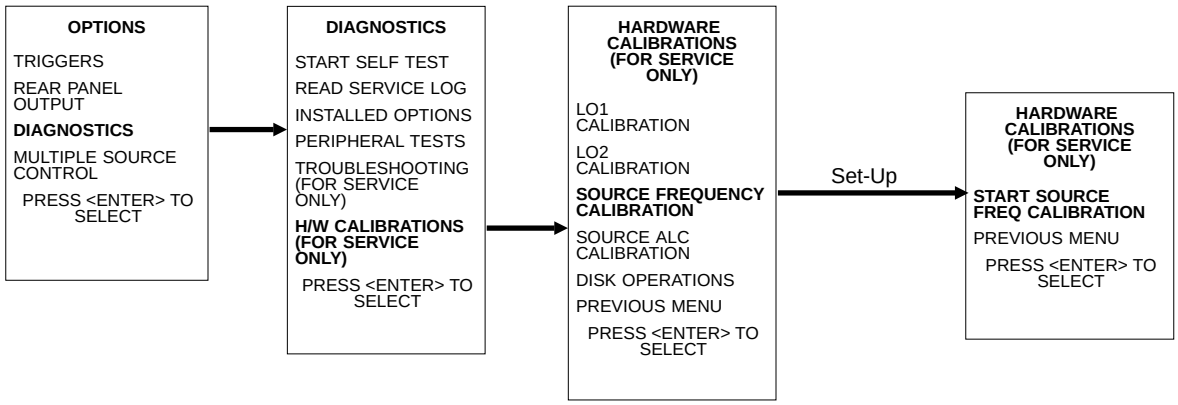
Step 6. Follow the directions displayed on the 371XXA CRT screen until calibration is completed.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:



Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu.Then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.ALC.**

NOTE

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type (FRE), date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

Step 3. Perform the Source FM/Lock Linearity test in Chapter 3, Operational Tests. If the test fails, proceed to Chapter 5, Troubleshooting.

If calibration fails:

- Verify that the frequency counter is functioning correctly, the cable is in good condition, and all connections are secure.
- Note which calibration step failed from the screen messages.
- Repeat the calibration. If it still fails, then proceed to Chapter 5, Troubleshooting.

6-5 RF POWER/ALC CALIBRATION

This procedure uses the 371XXA internal diagnostics and calibration menus, in conjunction with a suitable power meter, to adjust the output power level of the signal source throughout the range of the 371XXA model being calibrated. Perform this calibration procedure if:

- The Source Power/ALC test in Chapter 3, Operating Test, fails.

- Other testing or troubleshooting reveals a possible problem with RF Power accuracy or the ALC loop.
- Any of the following assemblies are replaced:
  - A21A1 Source YIG/Bias
  - A21A2 Source Controller
  - Down Converter
  - YIG Oscillator
  - Switched Filter
  - Power Splitter
  - SDM (37169A)
- BBRAM chip on the A9 Processor PCB is replaced and the Source Calibration Data was not previously saved on disk (thus data could not be recalled from disk).

Calibration Procedure

Perform the following steps:

Equipment Required

Refer to Table 1-1, located on page 1-8, for further information about the following equipment:

HP 437B Power Meter with HP 8487A Power Sensor

or:

Gigatronics 8541/8542 with 80304A Power Sensor

GPIB cable, ANRITSU 2100-2, or equivalent

NOTE

Allow the 371XXA and power meter to warm-up at least 30 minutes prior to performing calibration.

Procedure

Step 1. Connect test equipment as shown in Figure 6-2.

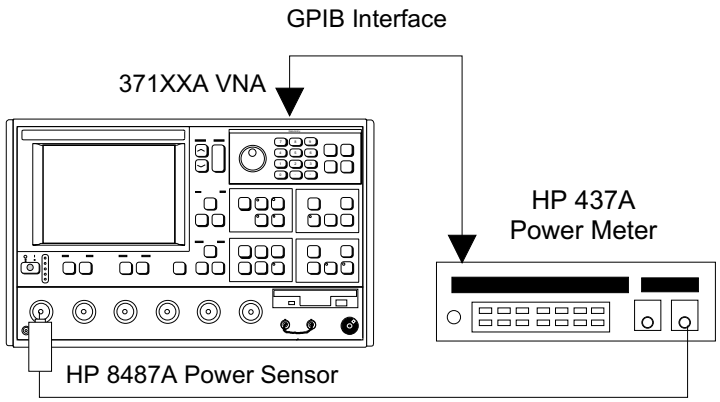
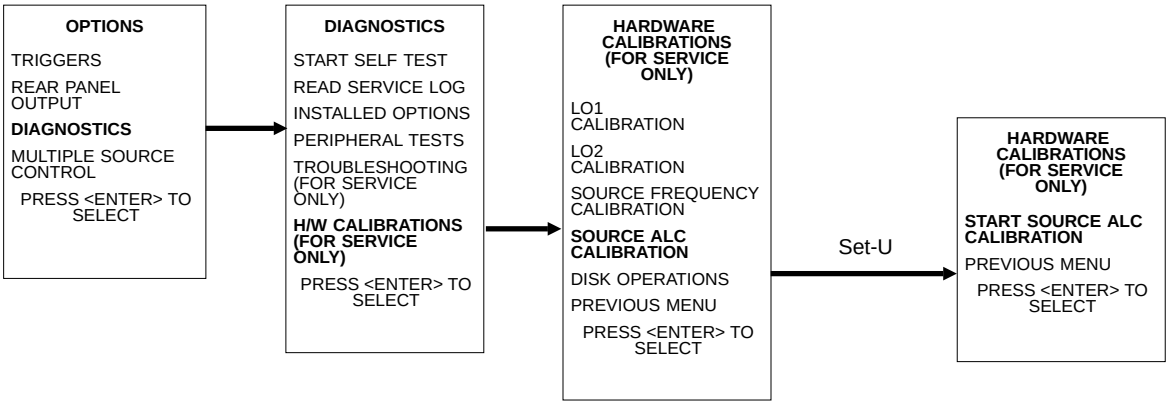


Figure 6-1. *Equipment Set-Up for RF Power/ALC Calibration*

Step 2. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 3. Select **DIAGNOSTICS** from menu; then select in sequence: **H/W CALIBRATIONS**, and then **SOURCE ALC CALIBRATION** (below).



Step 4. Follow the directions displayed on the screen to set-up and connect the power meter to the 371XXA.

Step 5. Select **START SOURCE ALC CALIBRATION** from menu.

Step 6. Follow the directions displayed on the 371XXA CRT screen, until calibration is completed.

Post Calibration Actions After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu.Then select in sequence: **H/W CALIBRATIONS |DISK OPERATIONS |SAVE TO HARD DISK|HW_CAL.ALC.**

NOTE

Also save the calibration data to floppy disk for archival purposes as a backup in case of a hard disk failure. Label the disk with calibration type (ALC), date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

Step 3. Perform the RF Power Generation and Control test in Chapter 3, Operational Tests. If the test fails, proceed to Chapter 5, Troubleshooting.

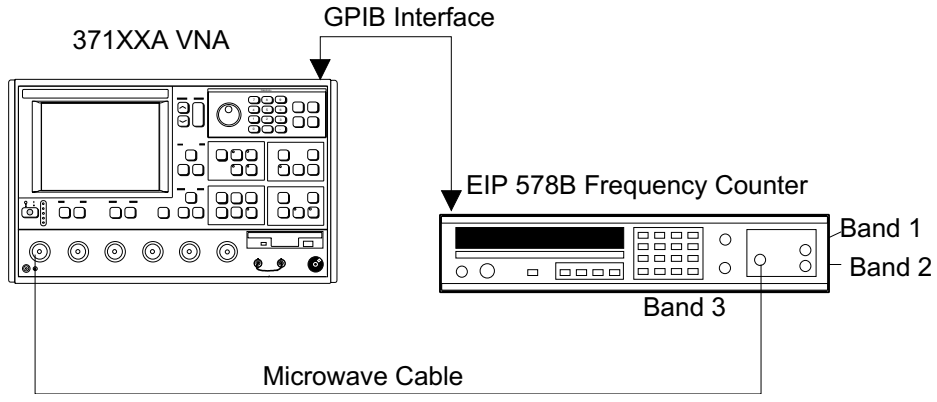


Figure 6-2. *Equipment Set-Up for Frequency Calibration*

If calibration fails:

Perform the following:

- Verify that the power meter and sensor are functioning correctly, the cables are in good condition, and all connections are secure.
- Verify the correct power sensor data exists in the power meter.
- Note the failed step in the calibration procedure from the screen messages.
- Repeat calibration. If it still fails then proceed to Chapter 5, Troubleshooting.

Chapter 7
System Description

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Chapter 7
System Description

7-1 INTRODUCTION

This chapter provides a brief overview of the functional assemblies and major parts that comprise a typical Series 37100A VNA system. It also briefly describes the operation of each major assembly.

7-2 SYSTEM OVERVIEW

Series 37100A Vector Network Analyzers are configured as Direct-Access Receivers for antenna, frequency conversion, and multiple output device measurements in the 22.5 MHz to 40 GHz frequency range. The 371XXA also maintains the ability to measure all four S-parameters with the addition of a reflectometer setup at the front end of the receiver.

The 371XXA performs these measurements by sourcing a stimulus signal to the Device Under Test (DUT) that is connected to the front panel RF Out connector. (See Figure 7-1 on page 7-5). It simultaneously measures the DUT response. The test signal(s) and a sample of the stimulus signal, are down converted and then transformed into their real and imaginary vector components. The resultant vector components are measured and converted into digital information. This digital information is sent to the Main Processor PCB where the desired data is processed and then presented to the user via the front panel color display. The display information is also sent to the rear panel VGA Out connector for use with an external VGA monitor.

The processed measurement information is also sent to the rear panel Printer Out connector for use with an external printer and/or plotter.

A front panel keypad, a rotary knob, and an IBM compatible keyboard interface provide user interaction with 371XXA Main Processor PCB.

The system is equipped with internal hard disk and floppy disk drives and battery backed internal memories for storage and retrieval of data and front panel setup information.

The 371XXA implements an IEEE 488.2 interface. This GPIB interface allows an externally connected instrument controller to control the 371XXA system in the “Remote-Only” mode. All 371XXA measurement and input/output operations may be controlled remotely in this mode.

An internal service log stores a record of system failures, data about the failures, and other key system service information. The service log is implemented using internal battery-backed SRAM memory.

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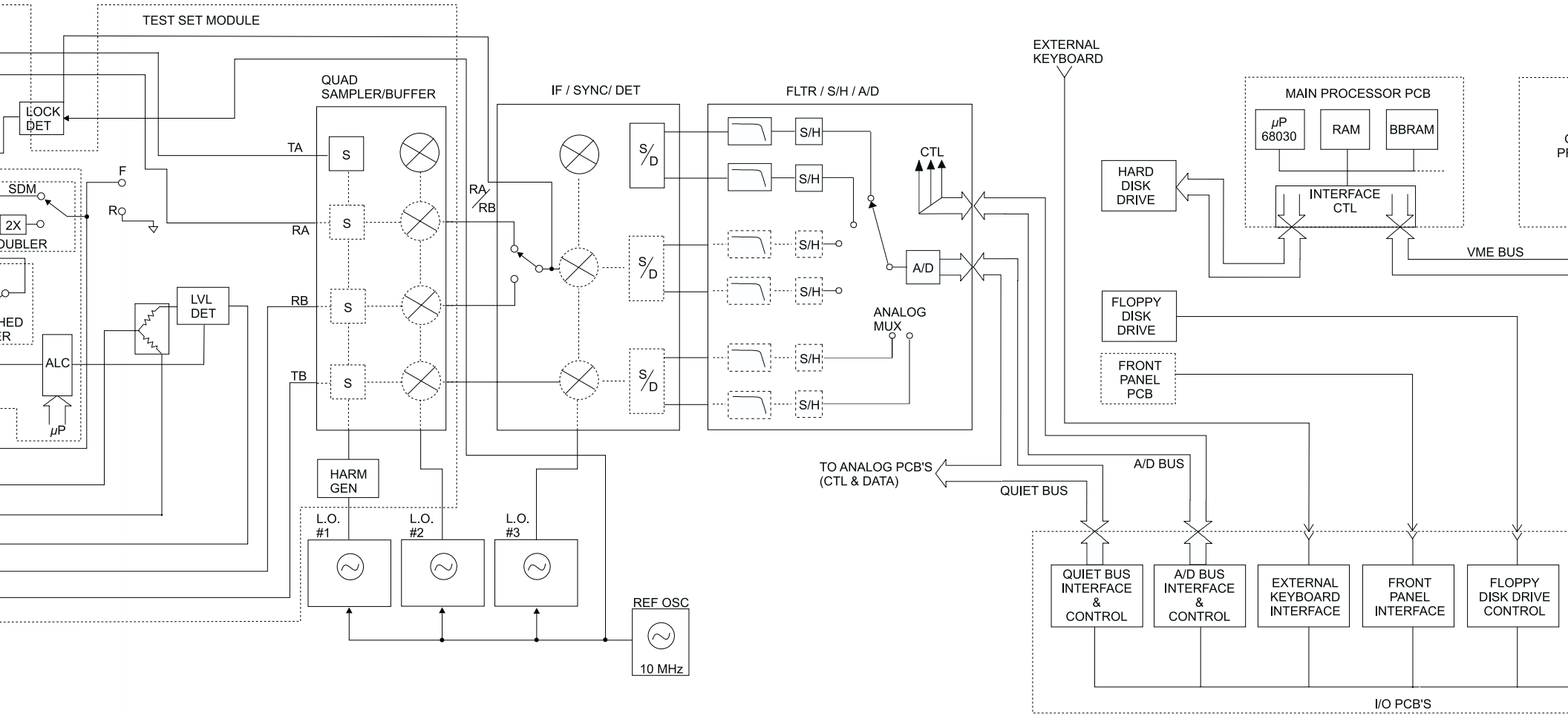
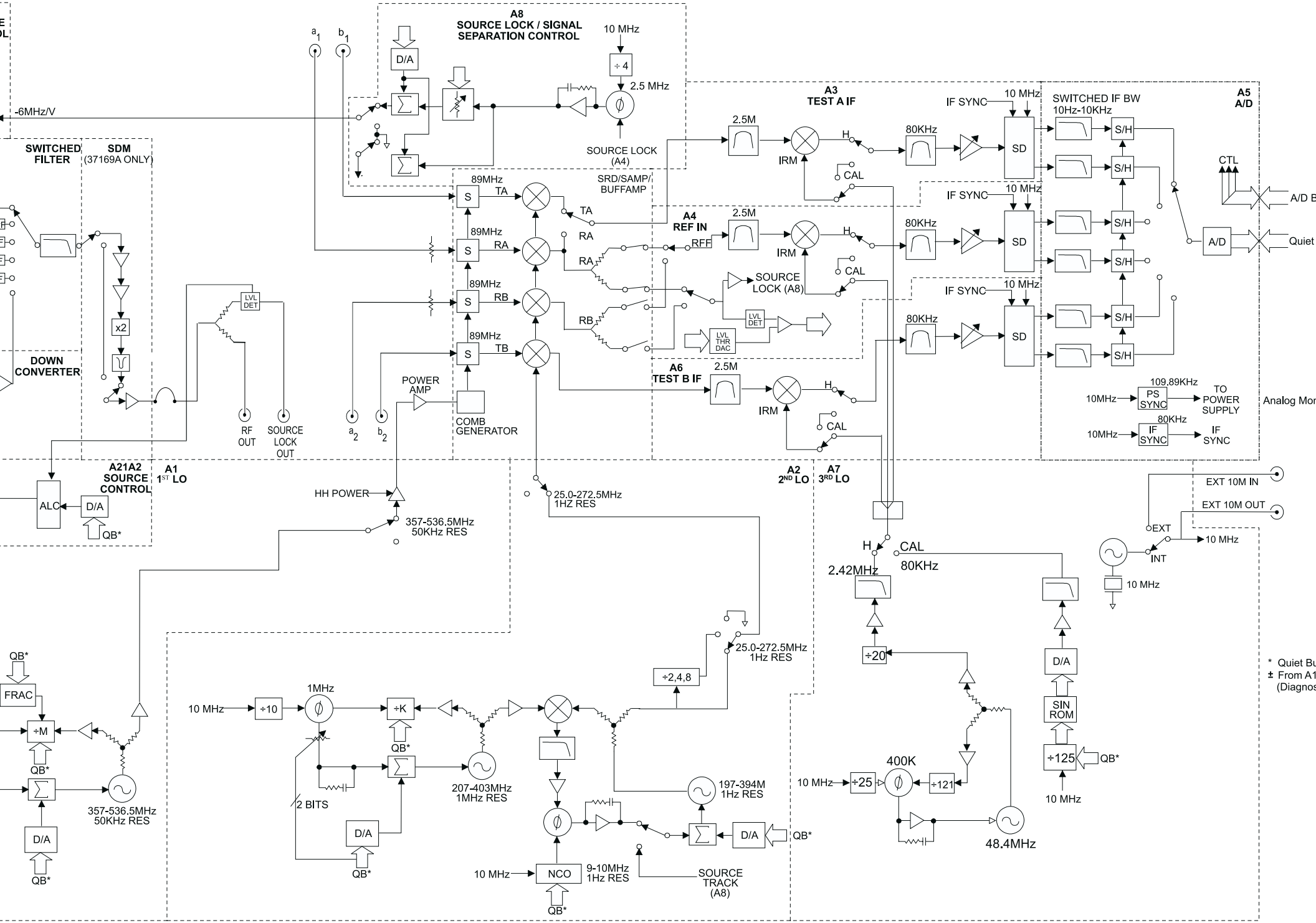

TEST SET MODULE
LOCK DET
SDM
2X
DOUBLER
F
R
ALC
µP
LVL DET
QUAD SAMPLER/BUFFER
TA
RA
RB
TB
S
RA/RB
IF / SYNC/ DET
S/D
FLTR / S/H / A/D
S/H
CTL
A/D
ANALOG MUX
HARM GEN
L.O. #1
L.O. #2
L.O. #3
REF OSC
10 MHz
TO ANALOG PCB'S (CTL & DATA)
QUIET BUS
A/D BUS
EXTERNAL KEYBOARD
MAIN PROCESSOR PCB
µP 68030
RAM
BBRAM
INTERFACE CTL
VME BUS
HARD DISK DRIVE
FLOPPY DISK DRIVE
FRONT PANEL PCB
QUIET BUS INTERFACE & CONTROL
A/D BUS INTERFACE & CONTROL
EXTERNAL KEYBOARD INTERFACE
FRONT PANEL INTERFACE
FLOPPY DISK DRIVE CONTROL
I/O PCB'S


A8
SOURCE LOCK / SIGNAL
SEPARATION CONTROL
10 MHz
÷ 4
2.5 MHz
D/A
SOURCE LOCK
(A4)
-6MHz/V
SWITCHED
FILTER
SDM
(37169A ONLY)
DOWN
CONVERTER
x2
LVL
DET
RF
OUT
SOURCE
LOCK
OUT
A21A2
SOURCE
CONTROL
A1
1ST LO
ALC
D/A
QB*
HH POWER
357-536.5MHz
50KHz RES
POWER
AMP
COMB
GENERATOR
SRD/SAMP/
BUFFAMP
89MHz
TA
RA
RB
TB
S
A3
TEST A IF
2.5M
IRM
H
CAL
IF SYNC
10 MHz
80KHz
SD
SWITCHED IF BW
10Hz-10KHz
S/H
A5
A/D
CTL
A/D B
Quiet
A4
REF IN
RFF
SOURCE
LOCK (A8)
LVL
THR
DAC
A6
TEST B IF
109.89KHz
PS
SYNC
TO
POWER
SUPPLY
Analog Mon
IF
SYNC
A2
2ND LO
A7
3RD LO
25.0-272.5MHz
1HZ RES
EXT 10M IN
EXT 10M OUT
EXT
INT
10 MHz
2.42MHz
÷20
÷2,4,8
FRAC
÷M
÷10
1MHz
÷K
2 BITS
207-403MHz
1MHz RES
197-394M
1Hz RES
400K
÷25
÷121
48.4MHz
SIN
ROM
÷125
NCO
9-10MHz
1Hz RES
SOURCE
TRACK
(A8)
* Quiet Bu
± From A1
(Diagnos

7-3 ANALOG SUBSYSTEM ASSEMBLIES

The following paragraphs briefly describe the major assemblies that comprise the 371XXA Analog Subsystem. Descriptions of the functions performed by each assembly are also included.

Signal Source Module

The Signal Source Module consists of the items listed below; refer to the block diagram of the Analog Subsystem (Figure 7-2) at left.

- 2-20 GHz YIG Oscillator Assembly
- A21A1 YIG/Bias Controller PCB
- A21A2 Source Control PCB
- Switched Filter Assembly
- Down Converter Assembly

The Signal Source Module is a swept frequency signal generator that produces a phase locked (and leveled) output signal within a range of 22.5 MHz to 20 GHz. All Series 371XXA VNA models employ phase-lock control of the signal source module so that the output frequency is accurate and stable. The output signal is phase locked by the
–6 MHz/volt control signal fed back from the A8 Source Lock/Separation Control PCB Assembly (which is described in following paragraphs).

All Series 371XXA VNA models use a single YIG-tuned oscillator to produce fundamental frequency source signals from 2.0 to 20 GHz. All other output frequencies are derived from the fundamental frequencies generated by the YIG-tuned oscillator. The signal source output frequencies for the low end portion of the frequency range (22.5 MHz to 2.0 GHz) are produced by down converting YIG fundamental signals in the range of 6.3225 to 8.3 GHz.

For Model 37169A, the signal source output frequencies for the high end portion of the frequency range (20 to 40 GHz) are produced by the Switched Doubler Module that doubles the YIG fundamental signals in the range of 10 to 20 GHz. The Switched Doubler Module (SDM) is located in the Test Set Module (described below.) The A21A2 Source Control PCB assembly provides all bias and control signals for the SDM.

The YIG-tuned oscillator generates a high-power RF output signal that has low broadband noise and low spurious content. The frequency of the YIG-tuned oscillator is controlled by means of :

- The YIG main tuning coil
- The YIG FM (fine tuning) coilThe system A9 Main Microprocessor PCB sends the data that represents the desired operating frequency to the A21A2 (Source Control) PCB, which converts the frequency data to analog signals. These signals are then sent to

the A21A1 YIG/Bias Controller PCB. This PCB converts the analog signals to YIG main tuning coil current.

The main tuning coil current from A21A1 YIG/Bias Controller PCB coarsely tunes the YIG-tuned Oscillator to within a few megahertz of the final output frequency. The YIG phase-lock loop then fine tunes the YIG-tuned oscillator to the exact output frequency via the FM (fine tuning) coil.

The fundamental frequency source signal is leveled by a PIN Diode attenuator that is part of the Switched Filter Assembly. This attenuator is controlled by the Automatic Leveling Control (ALC) circuits that are located on the A21A2 Source Control PCB. The input to the ALC circuits is the DC feed-back signal from the leveling detectors located in the Test Set Module.

Depending on the frequency of operation, the fundamental signal is passed through one of four low-pass filters located in the Switched Filter Assembly. The cut-off frequencies for these filters are 3.3 GHz, 5.5 GHz, 8.4 GHz, and 13.5 GHz, respectively. The signal is then passed through a 20 GHz high pass filter before being routed either directly to the Test Set Module, or to the Down-Converter Assembly .

The signal is switched to the Down-Converter Assembly only when the 371XXA is operating in the low end portion of its frequency range. The frequency of the output signal from the Down-Converter Assembly is 22.5 MHz to 2 GHz. The output signal from the Down-Converter Assembly is routed to the Test Set Module.

Test Set Module

The Test Set Module consists of the items listed below; refer to Figure 7-2.

- Level Detector
- Switched Doubler Module for 20-40 GHz operation (Model 37169A)

In the Test Set Module, the 22.5 MHz – 20 GHz signal from the signal source module is output to the DUT via the RF Out front panel connector.

The output circuit path contains a splitter. One path from the splitter goes to the RF OUTPUT connector and the other path feeds the associated level detector. The output generated by the level detector is a DC signal that corresponds to the output level of the stimulus signal. This signal is the input signal for the ALC circuits located in the signal source module.

The Test Set simultaneously receives front panel A1, B1, A2, B2 connectors device-under-test (DUT) signals via the couplers. These test signals are sent to the Receiver Module.

Receiver Module

The Receiver Module consists of the items listed below; refer to Figure 7-2.

- Quad Sampler/Buffer Amplifier with integrated SRD (step recovery diode)
- Power Amplifier
- A1, LO1 PCB
- A2, LO2 PCB

The Receiver Module is a four channel two stage Sampler/Buffer Amplifier and Down Conversion unit. It simultaneously converts the four 22.5 MHz - 40 GHz signals from the Test Set Module into three 2.5 MHz IF signals that are output to the IF Section.

The first stage of the Receiver Module uses harmonic sampling to down-convert the four 22.5 MHz – 40 GHz output signals from the Test Set Module down to 89 MHz signals. Any input signals below 270 MHz are passed directly through the four harmonic samplers to the second stage without down-conversion. The drive signal to each of the harmonic samplers is a comb of harmonics generated by a step recovery diode (SRD).

The Power Amplifier provides the signal that drives the SRD. The input to the Power Amplifier is the 357 – 536.5 MHz signal from the A1 First Local Oscillator (LO1) PCB. Regardless of the operating frequency, the Power Amplifier is biased on at all times to insure optimum thermal stability.

The second stage of the Receiver Module uses the 25.0 – 272.5 MHz signal from the A2 Second Local Oscillator (LO2) PCB to down-convert the 89 MHz signals into four 2.5 MHz IF signals TA, TB, RA, RB (two test signals and two reference signals). Either the Reference A or the Reference B IF signal is selected, as is appropriate for Forward/Reverse operation. The resultant three 2.5 MHz IF signals (Test A, Test B, and Reference A/B) are output to the IF Section. A buffered version of the Reference A/B signal is also fed to the A8 Source Lock/Signal Separation Control PCB as the Source Lock signal.

The Receiver Module can also select the Reference A IF signal that is output to the IF Section via the Test A switch path. This IF signal is used during Line Reflect Line (LRL) Calibrations to ratio the Reference A and Reference B signals.

A8, Source Lock/ Signal Separation and Control PCB

The Source Lock Phase Comparator circuit on the A8 Source Lock/ Signal Separation Control PCB compares the Source Lock (Reference A/B) signal from the Receiver Module with a signal derived from the 10 MHz reference oscillator. The output of this circuit is the –6 MHz/V correction signal, which is routed to the circuit on the A21A2 Source Control PCB that generates the FM coil tuning current signal. This signal is output to the A21A1 YIG/Bias Controller PCB to fine tune the YIG-tuned oscillator to the exact output frequency. When the YIG-tuned oscillator outputs the exact frequency, the two inputs to the phase comparator circuit on the A8 PCB match and the phase-lock loop is locked.

The A8 PCB Assembly also provides bias and control signals to the Test Set and Receiver Modules for operating the following circuits:

- Power Amplifier
- Quad/Sampler Buffer Amplifier
- Step Attenuators (External)

IF Section

The IF Section consists of the items listed below; refer to Figure 7-2.

- A3 Test A IF PCB
- A4, Reference IF PCB
- A5, A/D Converter PCB
- A6, Test B IF PCB
- A7, Third Local Oscillator, LO3, PCB

The IF Section converts the three 2.5 MHz IF signals from the Receiver Module into six DC output signals. The A3 (Test A), A4 (Reference A/B), and A6 (Test B) PCBs down-convert the 2.5 MHz input IF signals to 80 kHz IF signals and then adjust their amplitude for input to the synchronous detector stage of each PCB. Each 80 kHz IF signal is synchronously detected and converted into a pair of DC signals that contain the information for the real and imaginary portions of the original 80 KHz IF signal. Thus, the three IF signals (two test signals and the reference signal) yield six DC signals that fully represent the real and imaginary vector components of the DUT's S-parameters.

The IF Section also checks the 2.5 MHz phase lock signal for proper power level by comparing it to a known reference level on the A4 PCB. A sample of the 2.5 MHz Reference A/B IF signal is sent to the A8 Source Lock/Separation Control PCB assembly for phase locking the signal source module. The A3 and A6 PCBs are functionally identical and physically interchangeable.

A7 PCB, LO3

The A7, Third Local Oscillator (LO3) Assembly, provides a fixed 2.42 MHz Local Oscillator signal that is used on the A3, A4, and A6 PCBs to down-convert the 2.5 MHz IF signals to 80 kHz. It also provides an 80 kHz standard signal for the IF Section Calibration process that occurs au-

tomatically approximately every six minutes. This automatic IF Section Calibration is one of the 371XXA features that ensures rated measurement accuracy. Automatic IF Calibration can be turned off and/or invoked at any time during measurement sweeps.

A5 A/D Converter PCB

The A5 A/D Converter PCB contains a six-channel, two stage, switched-filter sample-and-hold circuit and a 20 bit A/D converter. Each of the six DC signals from the A3, A4, and A6 PCBs are input to a separate channel of the PCB. The first stage of each channel is a low-pass filter with four selectable cutoff frequencies of 10 kHz, 1 kHz, 100 Hz, and 10 Hz. The second stage of each channel is a sample-and-hold amplifier that stores the signals during the A/D conversion process. Each channel is sequentially selected for input to the 20 bit A/D converter.

The A5 A/D Converter PCB also derives the 109.89 kHz Power Supply Synchronization Signal and the 80 kHz IF Synchronization Signal from the 10 MHz Reference Timebase. Additional functions of the A5, A/D Converter Assembly include:

- Measurement of power supply voltages and other internal nodes of the 371XXA for diagnostic purposes.
- Measurement of an externally applied analog input signal. This function is used for service purposes only.
- External Trigger Input signal processing (from rear panel)
- External Analog Output signal generation (to rear panel)

The A/D converter circuitry located on the A/5 PCB is used as a DVM to measure various internal system analog monitor points on the A1 – A8 and A21A1/ A21A2 PCBs. It is also used to monitor power supply voltages and other critical points throughout the 371XXA, which can be readout via the Diagnostics Menus. DVM readings are also recorded in the service log for certain system failures.

7-4 DIGITAL SUBSYSTEM ASSEMBLIES

The following paragraphs briefly describe the major assemblies that comprise the 371XXA Digital Subsystem. The digital subsystem provides all system control, I/O interface, digital signal processing, and data presentation functions.

The major assemblies that comprise the 371XXA digital PCB subsystem are listed below. Refer to Figure 7-3, at left.

- A9, Main Processor PCB
- A13, I/O Interface #1 PCB
- A14, I/O Interface #2 PCB
- A15, Graphics Processor PCB
- A16, Hard Disk PCB
- A18, Rear Panel Interface
- Rear Panel Assembly
- Front Panel Assembly
- Floppy Disk Assembly
- A24, VME Bus Terminator PCB

A9 Main Processor PCB Assembly

The major components that comprise the A9 Main Processor PCB are:

- 68040 Microprocessor (w/ integrated co-processor) – This is the CPU for the 371XXA system.
- 4 MB DRAM – This is the main system memory. This memory is volatile (non-battery backed). During normal operation, it stores the 371XXA software that is loaded from disk at power-up.
- 8 KB BBRAM – This auxiliary memory chip contains a back-up battery that is continuously recharged whenever power is applied. (The back-up battery has a four year minimum life span.) This chip also contains real time and date clock functions. It is used to store low level boot-up parameters, ALC calibration data, source frequency calibration data, and service log header data.
- 512 KB SRAM – This auxiliary memory is backed-up by a non-rechargeable Lithium battery that provides 200 days (maximum) of power-off protection. It is used to store current and saved front panel setups, trace/normalization data, current RF calibration data, current sweep frequency data, flat power calibration data, and the service log error list.
- VME Bus interface chip – This chip is used to interface the Main Processor PCB to the A13, A14, and A15 digital PCBs (via the VME bus interface).
- SCSI Bus interface – This chip is used to interface the Main Processor PCB to the A16 Hard Disk PCB.

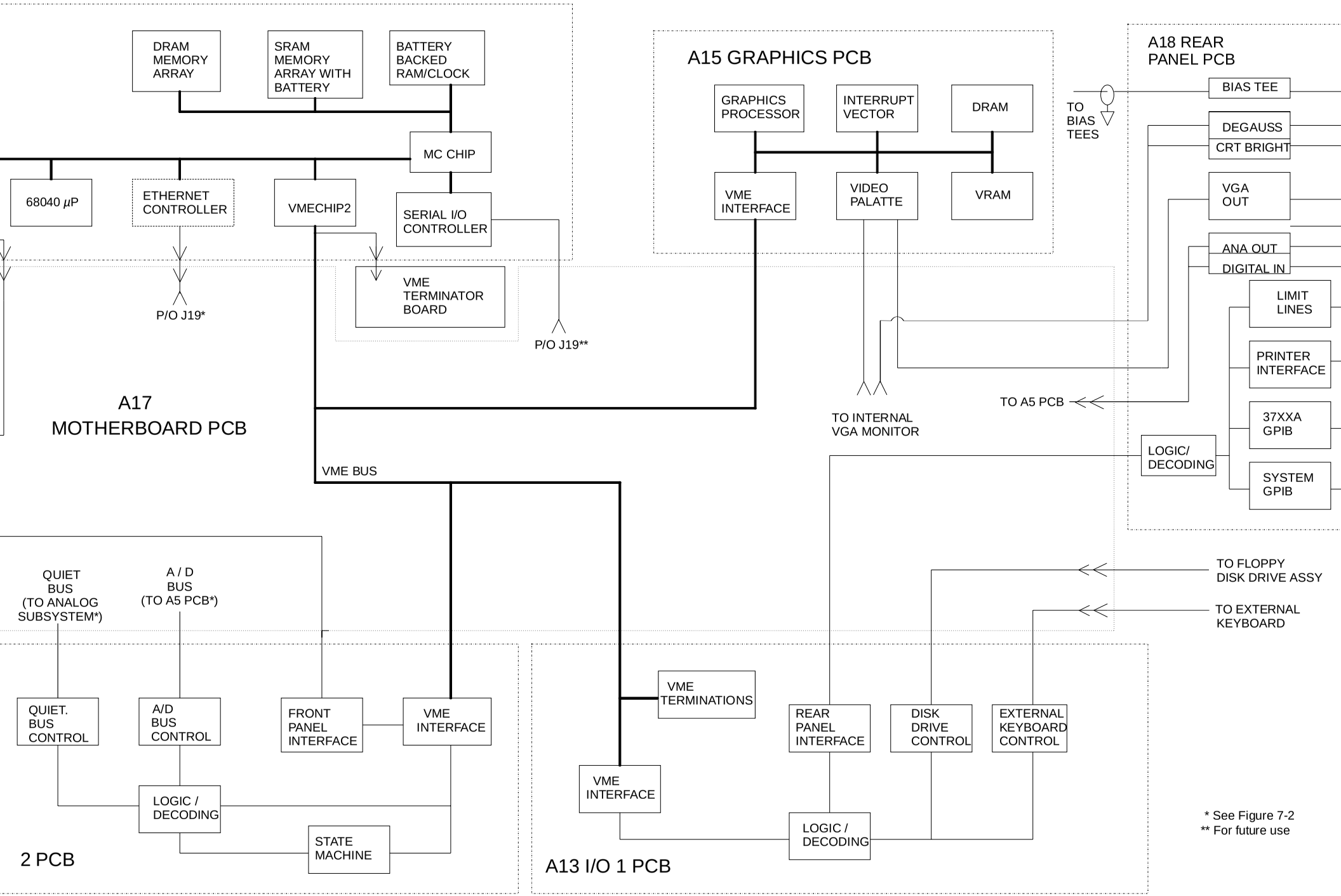
- System boot-up EPROM – This chip contains the boot-up instructions used by the system CPU at power-up.

A7 PCB, 10 MHz Timebase

Except for units equipped with Option 10, the A7 PCB contains the 10 MHz TCXO Reference Timebase that is the master timebase for the system. It also contains the signal distribution and switching functions for all External/Internal 10 MHz reference signals.

The A7 PCB provides the fixed 2.42 MHz Local Oscillator signal and the 80 kHz Calibration signal to the IF PCBS (A3, A4, and A6). These signals are derived from the 10 MHz Reference Timebase.

- Units equipped with Option 10 have a high-stability ovenized timebase mounted inside the rear panel directly above the Power Supply Module. This timebase replaces the standard 10 MHz timebase located on the A7 PCB. The output from this timebase is routed to the A7 PCB for distribution. It is powered by regulated +24 vdc from the A7 PC


DRAM MEMORY ARRAY
SRAM MEMORY ARRAY WITH BATTERY
BATTERY BACKED RAM/CLOCK
MC CHIP
68040 μP
ETHERNET CONTROLLER
VMECHIP2
SERIAL I/O CONTROLLER
VME TERMINATOR BOARD
P/O J19*
P/O J19**
A17 MOTHERBOARD PCB
A15 GRAPHICS PCB
GRAPHICS PROCESSOR
INTERRUPT VECTOR
DRAM
VME INTERFACE
VIDEO PALATTE
VRAM
TO BIAS TEES
TO INTERNAL VGA MONITOR
A18 REAR PANEL PCB
BIAS TEE
DEGAUSS
CRT BRIGHT
VGA OUT
ANA OUT
DIGITAL IN
LIMIT LINES
PRINTER INTERFACE
37XXA GPIB
SYSTEM GPIB
TO A5 PCB
LOGIC/ DECODING
VME BUS
QUIET BUS (TO ANALOG SUBSYSTEM*)
A / D BUS (TO A5 PCB*)
TO FLOPPY DISK DRIVE ASSY
TO EXTERNAL KEYBOARD
QUIET. BUS CONTROL
A/D BUS CONTROL
FRONT PANEL INTERFACE
VME INTERFACE
LOGIC / DECODING
STATE MACHINE
2 PCB
VME TERMINATIONS
VME INTERFACE
REAR PANEL INTERFACE
DISK DRIVE CONTROL
EXTERNAL KEYBOARD CONTROL
LOGIC / DECODING
A13 I/O 1 PCB
* See Figure 7-2
** For future use

A13 I/O Interface #1 PCB Assembly

This PCB assembly performs the following functions:

- Floppy drive control – interface for the Floppy Drive Assembly.
- External Keyboard control – interface for the front panel Keyboard connector.
- Interface for the A18 Rear Panel PCB Assembly (below).
- Interface and control for the rear panel IEEE 488.2 GPIB and Dedicated GPIB interface connectors.

A14 I/O Interface #2 PCB Assembly

This PCB assembly contains a State Machine controller, decode logic, and bus interface control circuits that perform the following functions:

- Quiet Bus interface control. The Quiet Bus passes control and data signals from the A9 Main Processor PCB to the A1 – A8, and A21 PCBs and returns status and data signals back to the A9 PCB. This bus is managed by the control circuits on the A14 PCB such that it is inactive during the the time that a measurement is being taken.

  NOTE

  The output data from the A5 PCB A/D converter is sent to the A9 Main Processor PCB via the Quiet Bus, the A14 PCB, and the VME Bus.

- A/D Bus interface control. During the measurement process, all A/D selection and conversion functions on the A5 PCB are controlled exclusively by the A14 PCB State Machine Controller. This is accomplished via the command lines of the A/D Bus.
- Measurement control functions – the A14 PCB State Machine Controller manages many of the 371XXA functions during a measurement, as follows:
  - Quiet Bus interface control
  - A/D Bus interface control:
    - Sample and Hold control for A5 PCB
    - A/D selection and conversion control for A5 PCB
  - Check for phase lock condition
  - Gain ranging
  - Delay generation for IF Bandwidth setting function

The A14 PCB also provides the interface to the Front Panel A19 and A20 PCBs

A15 Graphics Processor PCB Assembly

This PCB assembly contains circuitry that simultaneously drives both the internal VGA monitor and an external VGA monitor (if used), as follows:

- It receives measurement and display information from the A9 Main Processor PCB and generates screen display (video) information.
- Provides interface and control for the internal VGA Monitor Assembly.
- Provides interface for an external monitor via the rear panel VGA Out connector.

A16 Hard Disk PCB Assembly

The PCB assembly contains a pre-formatted hard disk drive assembly and associated interface circuitry. The A16 PCB interfaces directly with the A9 Main Processor PCB via the (A9) SCSI interface.

Floppy Disk Drive Assembly

This unit is a standard 1.44 MByte DOS compatible format floppy disk drive. It is physically mounted to the test set tray (not to the Front Panel Assembly). It interfaces to the system via the A13 I/O Interface #1 PCB.

A24 VME Bus Terminator PCB

This PCB assembly terminates the VME bus to insure stable digital data transfer on the bus. It plugs into the VME bus structure on the bottom surface of the A17 Motherboard Assembly.

7-5 MAIN CHASSIS ASSEMBLIES

The assemblies described below are the major assemblies mounted to the basic frame of the 371XXA.

A17 System Motherboard Assembly

The motherboard assembly provides signal routing and D.C. power distribution paths for all major PCB assemblies of the Analog Subsystem (A1 – A8) and the Digital Subsystem (A9 – A16). It also contains the VME Bus, Quiet Bus, and A/D Bus structures and other signal routing paths. It does not contain any active components.

NOTE

The motherboard assembly is an integral part of the 371XXA chassis. It is not a field replaceable unit.

Front Panel Assembly

The Front Panel Assembly consists of the following assemblies and parts:

- A19 Front Panel Switch PCB – this assembly contains all of the front panel switches for the 371XXA VNA.
- A20 Front Panel Control PCB – this assembly contains the decode logic for the switches located on the A19 Front Panel Switch PCB. This PCB interfaces with the A14 I/O Interface #2 PCB Assembly.
- Front Panel LEDs, beeper, keys, controls, and connectors
- Front panel overlay
- Front panel casting

NOTE

The front panel is an integrated assembly that is replaceable only as a single unit.

Rear Panel Assembly

The Rear Panel Assembly includes the following rear panel connectors:

- 10 MHz Reference In and Out BNC connectors
- External Trigger BNC connector
- External Analog Input BNC connector
- External Analog Output BNC connector

This assembly also includes:

- Bias Tee fuses
- Reference Channel Extension Loops (Option 11)
- Main system fan
- The A18 Rear Panel PCB and associated connectors, circuitry, and cables (below).

A18 Rear Panel Interface PCB

This PCB assembly contains the rear panel connectors listed below. It also includes the associated circuitry and cabling interfaces that link these connectors (and the rear panel fan assembly) to the A17 Motherboard PCB and other assemblies within the 371XXA.

- IEEE 488.2 GPIB connector (with associated interface circuits)
- Dedicated GPIB connector (with associated interface circuits)
- Printer Out connector (with associated interface circuits)
- VGA Out connector
- CRT degauss and brightness controls
- I/O Connector (and associated interface circuits)– This 25 pin miniature D-sub connector contains:
  - Limits Testing Status TTL outputs
  - Ext Dig In signal (same as External Trigger BNC)
  - Ext Ana Out signal (same as External Analog Output BNC)

The A18 PCB also contains:

- Routing of –27 Vdc power to the rear panel system fan.
- Routing of External Analog Out and External Trigger Input signals to the Mother Board.

Power Supply Module

The Power Supply Module is a single self contained assembly mounted on the rear panel. This module provides:

- Unregulated +5, +9, ±18, and ±27 Vdc supply voltages to the other assemblies of the 371XXA.
- Dedicated AC line connection for the Internal VGA Monitor.
- Thermal and over-current shutdown protection circuitry
- Sensing and input power regulation for operation with 85 – 264 VAC, 48 – 63 Hz, universal AC line input power.
- Internal fan cooling (for power supply module)
- Supply voltages distribution

Table 7-1 identifies all 371XXA DC power supply voltages and lists their usage by the various PCB assemblies. Unless otherwise indicated, supply voltages are regulated on the assembly using them. The analog and digital power supply grounds are isolated.

NOTE

All power supply voltages listed in Table 7-1 can be accessed via the A/D bus for measurement by the the A/D converter circuitry (e.g., DVM) located on the A5 A/D PCB assembly.

Table 7-1. *371XXA Power Supply Voltages and Usages*

Internal VGA Monitor The internal monitor assembly is powered from a dedicated AC Line from the Power Supply Module. The degaussing and brightness controls for the internal monitor are located on the rear panel for easy access by the operator. There are no internal adjustments for this unit.

NOTE

The internal monitor assembly is not a field repairable unit.

Internal LCD Monitor The internal LCD is powered from the A17 Motherboard via a flexible PCB assembly. There are no internal adjustments for this unit.

NOTE

The LCD is not a field repairable unit.

Chapter 8
Remove and Replace Procedures

Table of Contents

Chapter 8
Remove and Replace Procedures

8-1 INTRODUCTION

This chapter provides procedures for removing and replacing 371XXA field exchangeable assemblies and components. When using these procedures, please observe the warning and caution notices below.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels.

CAUTION

Many assemblies in the 371XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

8-2 EQUIPMENT REQUIRED

All procedures in this chapter require the use of either a #1 or #2 size Phillips type screw driver. Any additional tool requirements are specified at the beginning of each procedure.

8-3 REMOVE / REPLACE 371XXA COVERS

Adjustment and troubleshooting operations require removal of the top cover. Replacement of some 371XXA assemblies and parts require removal of all covers. The following procedures describe this process.

NOTE

It is only necessary to loosen the 371XXA handle assemblies to remove the top, bottom, or side covers. However, if the front panel is to be removed, remove the handle assemblies at this time.

Preliminary:

❑ Switch the 371XXA power **off**. Remove the power cord.

Procedure:

Step 1. Loosen (or remove) the right and left handle assemblies, as follows:

- Place the 371XXA on its top (bottom-side up).
- Loosen/remove the screws at the sides of the handle assemblies.
- If removing handles, pull them away from unit and set aside.

CAUTION

The green headed screws have Metric threads.

Step 2. To remove the top cover:

- Place the 371XXA in normal (top-side up) position.
- Remove the feet from the two top corners at the rear of the 371XXA (Figure 8-1).
- Remove the center screw from rear of the top cover.
- Lift and slide the top cover away from the 371XXA.

Step 3. To remove the bottom cover:

- Place the 371XXA on its top (bottom-side up).
- Remove the feet from the two bottom corners at the rear of the 371XXA.
- Remove the center screw from rear of the bottom cover.
- Lift and slide the top cover away from the 371XXA.

Step 4. To remove the left cover:

- Place the 371XXA on its right side (monitor down).
- If not already done, remove the feet from the two left-side corners at the rear of the 371XXA.
- Remove two center screws from the left cover.
- Remove the center screw from rear of the left side cover.
- Lift and slide the side cover away from the 371XXA.

Step 5. To remove the right cover:

- Place the 371XXA its left side (monitor up).
- If not already done, remove the feet from the two right-side corners at the rear of the 371XXA.
- Remove the center screw from rear of the right side cover.
- Remove the center screw from rear of the right side cover.
- Lift and slide the side cover away from the 371XXA.

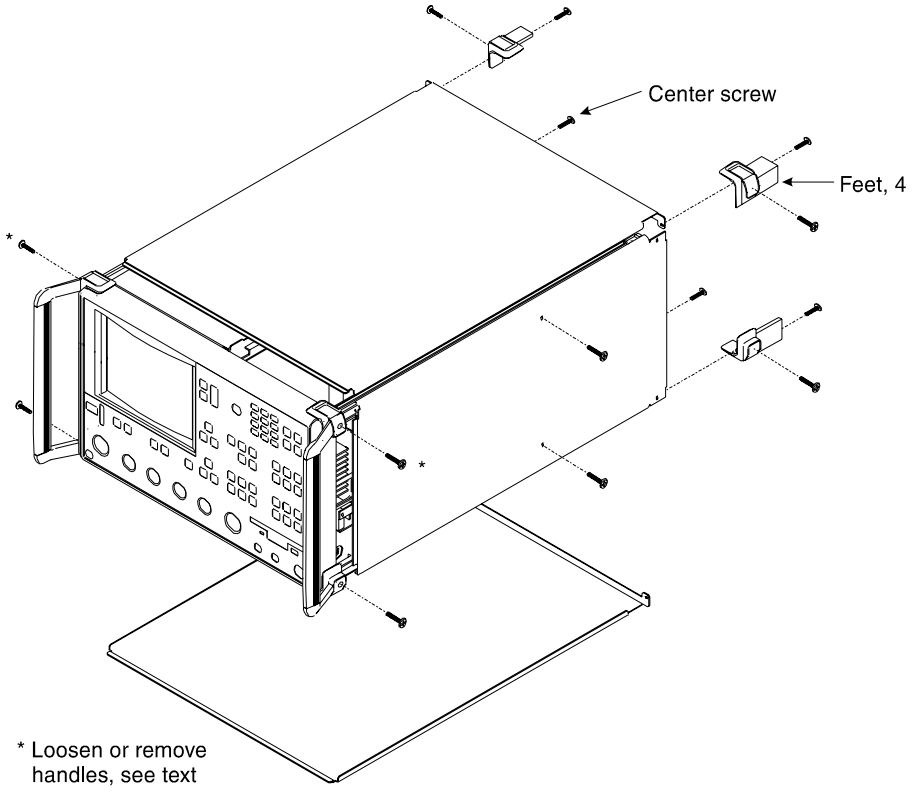


Figure 8-1. *Exploded View of 371XXA Chassis Covers*

To replace the instrument covers, perform the steps above in the reverse order.

8-4 REMOVE / REPLACE THE A1–A9 AND A13–A16 PCBS

This paragraph provides instructions for removing and replacing the A1– A9 and A13 – A16 PCB's, which are located underneath the covers of the large and small card-cages, respectively.

Preliminary:

- ❑ Switch the 371XXA power **off**. Remove the power cord.

Remove the top cover (paragraph 8-3).

A1 – A9 PCBs

Procedure:

Step 1. Place the 371XXA in normal (top-side up) position.

Step 2. Remove the two screws that secure the large card-cage cover (Figure 8-2).

Step 3. Remove the large card-cage cover and set aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight up.

To replace the PCB(s) and covers, perform the steps above in the reverse order.

A13 – A16 PCB's

Procedure:

Step 1. Place the 371XXA in normal (top-side up) position.

Step 2. Remove the two screws that secure the large card-cage cover (Figure 8-2).

Step 3. Remove the large card-cage cover, then remove the small card-cage cover and set aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight up.

To replace the PCB(s) and covers, perform the steps above in the reverse order.

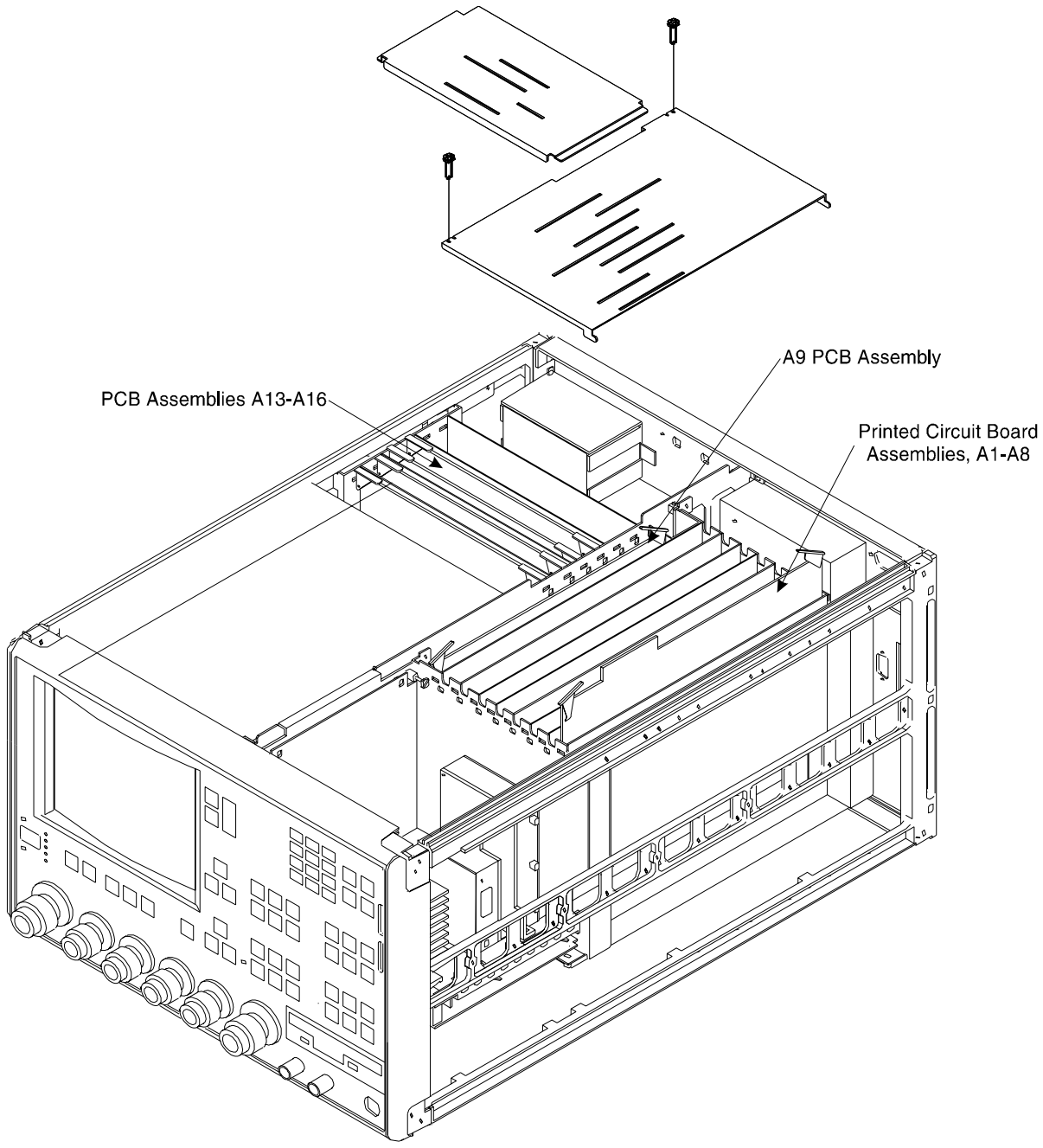


Figure 8-2. *A1-A9 and A13-A16 PCB Assemblies Removal Diagram*

8-5 REMOVE / REPLACE A9 PCB BBRAM CHIP

This paragraph provides instructions for removing and replacing the BBRAM Chip located on the A9 Main Processor PCB assembly.

Preliminary:

Before removing and replacing the BBRAM Chip it is necessary to save the following calibration data to the hard disk: signal source Frequency, ALC, LO1, and LO2. Proceed as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu (left).

Step 2. Select DIAGNOSTICS from the menu. Then select in sequence: H/W CALIBRATIONS |DISK OPERATIONS |SAVE TO HARD DISK |HW_CAL.ALL.

NOTE

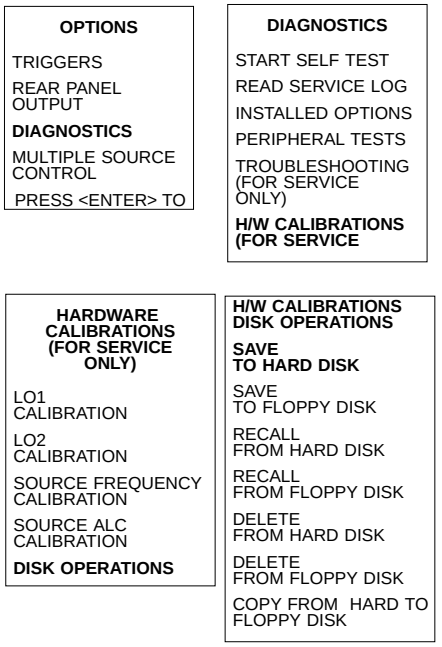
Also save the calibration data to floppy disk. Label the disk with calibration type (ALL), date, and system model and serial numbers. Set the copy protect tab on the disk. Properly safeguard the disk so that it will be available for later use, as needed.

Step 3. Switch the 371XXA power **off**. Remove the power cord.

Remove/Replace Procedure:

Step 1. Remove the top cover and the large card-cage cover to expose the A1 – A9 PCBs (refer to paragraph 8-3).

Step 2. Remove the A9 PCB from the unit.



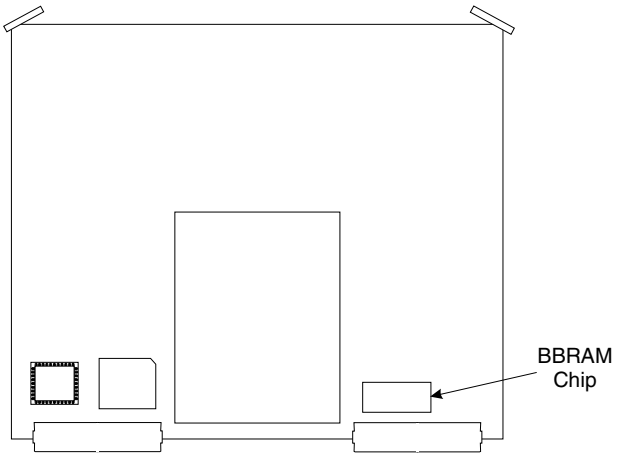
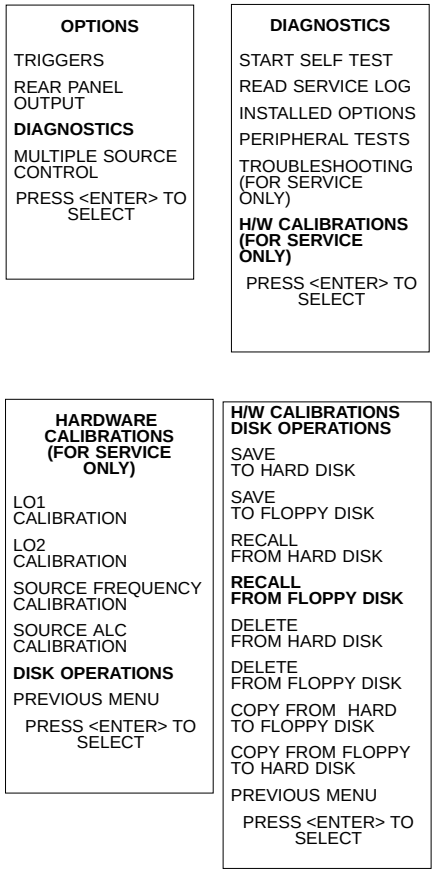


Figure 8-3. *Location of BBRAM Chip on the A9 PCB*



Step 3. Locate and remove the BBRAM chip from the A9 PCB. See Figure 8-3.

Step 4. Replace the BBRAM chip on the A9 PCB.

Step 5. Reinstall the A9 PCB, the large card-cage cover, and the top cover.

Step 6. Reconnect power cord. Switch 371XXA power **on**.

Post Replacement Procedure:

Recall the calibration data saved in the Preliminary step from the floppy disk as follows:

Step 1. Insert the floppy disk with the previously saved Source Frequency and ALC Calibrations Data in the 371XXA floppy disk drive.

Step 2. Select DIAGNOSTICS from the menu (left). Then select in sequence: H/W CALIBRATIONS | DISK OPERATIONS | RECALL CAL FROM FLOPPY DISK | HW_CAL.ALL.

NOTE

If unable to recall calibrations from disk, you must redo the calibration data described in the Preliminary step on the preceeding page.

Step 3. Ensure the system sweeps several times without errors.

Step 4. Refer to Chapter 3, Operational Tests. Perform the following:

- Check the Service Log for any new errors. (Note that the service log is non-volatile; it may contain error entries from a previous problem or service operation.)
- Run the Self Test procedure.
- Refer to Chapter 5, Troubleshooting, if any system errors are reported.

8-6 REMOVE / REPLACE A9 PCB SRAM BATTERY

This paragraph provides instructions for removing and replacing the SRAM Battery located on the A9 Main Processor PCB assembly.

Preliminary:

❑ Switch the 371XXA power **off**. Remove the power cord.

CAUTION

The SRAM battery incorporates flammable materials such as lithium and organic solvents. If lithium batteries, such as this one, are mistreated or incorrectly handled, they may *burst open and ignite.* This can result in possible injury or fire. When handling the SRAM battery, carefully following the following precautions:

- DO NOT short circuit.
- DO NOT disassemble, deform, or apply excessive pressure.
- DO NOT heat or incinerate.
- DO NOT apply solder directly.
- DO NOT mix model or new and old batteries.
- DO NOT charge.
- ALWAYS check that proper polarity is observed.

Remove/Replace Procedure:

Step 1. Remove the top cover and the large card-cage cover to expose the A1 – A9 PCBs (refer to paragraph 8-3).

Step 2. Remove the A9 PCB from the unit.

Step 3. Locate and carefully remove the SRAM battery from the A9 PCB. See Figure 8-4.

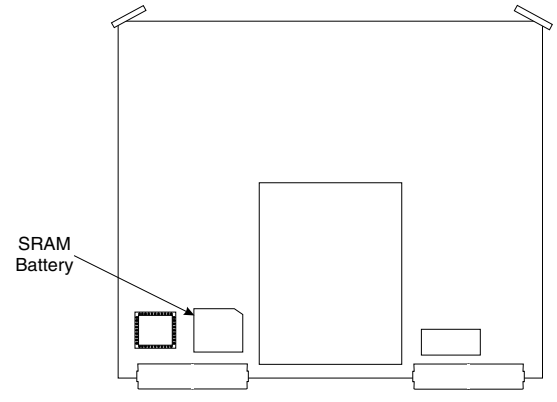
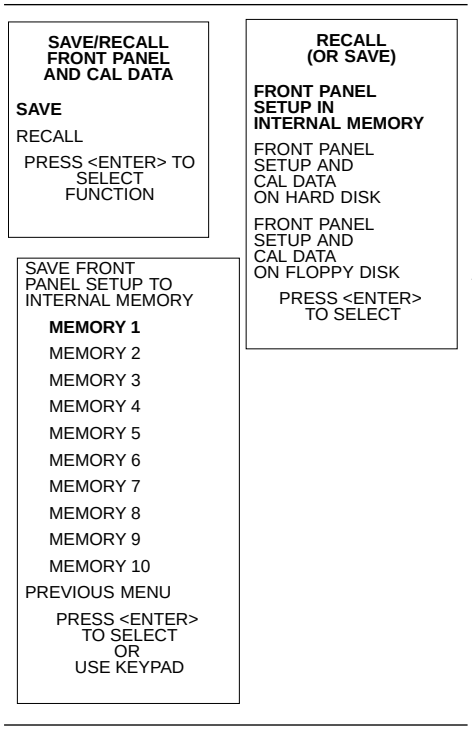


Figure 8-4. *Location of SRAM Battery on the A9 PCB*



Step 4. Replace the SRAM battery on the A9 PCB, as follows:
- Insure that the pins are clean.
- Note the polarity and carefully press the batterly into the socket.

Step 5. Reinstall the A9 PCB, the large card-cage cover, and the top cover.

Post Replacement Procedure:

Step 1. Connect power cord. Switch 371XXA power **on**.

Step 2. Ensure the system sweeps several times without errors.

Step 3. Refer to Chapter 3, Operational Tests. Perform the following:

- Check the Service Log for any new errors. (Note that the service log is non-volatile; it may contain error entries from a previous problem or service operation.)
- Run the Self Test procedure.
- Refer to Chapter 5, Troubleshooting, if any system errors are reported.

Step 4. Use front panel keys to set to Dual Channel Display 1 & 3.

Step 5. Save front panel setup to memory as follows:

- Press the Save/Recall Menu key
- Select SAVE from menu (top left): then in sequence select: FRONT PANEL SETU TERNAL MEMORY |MEMORY 1

Step 6. Reset system to default settings by pressing the Default key.

Step 7. Ensure the system resets to back to the default Quad-Channel display. Refer to Chapter 5, Troubleshooting, if it does not.

Step 8. Recall the saved memory 1 setup as follows:

- Press the Save/Recall Menu key
- Select RECALL from menu (bottom left): then in sequence select: FRONT PANEL SETUP IN INTERNAL MEMORY |MEMORY 1

Step 9. Ensure that the system recalls the previously saved Dual Channel Display 1 & 3. Refer to Chapter 5, Troubleshooting, if it does not.

8-7 REMOVE / REPLACE A24 VME BUS TERMINATOR PCB

This paragraph provides instructions for removing and replacing the A24 VME Bus Terminator PCB assembly.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove bottom cover (paragraph 8-3).

Remove/Replace Procedure

Step 1. Place the 371XXA on its top (bottom-side up).

Step 2. Locate the A24 PCB assembly (Figure 8-5). Unplug A24 PCB assembly from the A17 Motherboard PCB by gently pulling straight up on each side.

CAUTION

Be careful not bend or disturb the hard co-ax lines located near right edge of A24 PCB.

To replace the A24 PCB assembly, perform the steps above in the reverse order.

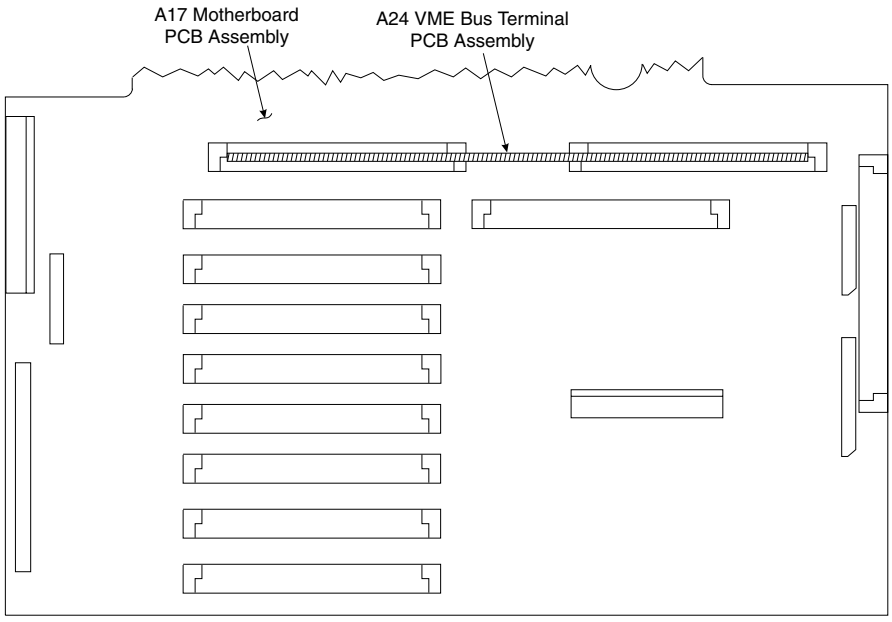
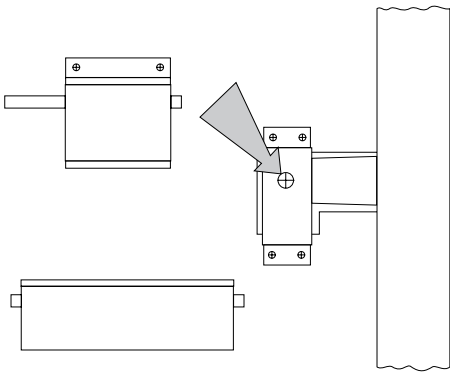


Figure 8-5. *Location of the A24 VME Bus Terminator PCB Assembly*

8-8 REMOVE / REPLACE FRONT PANEL ASSEMBLY



This paragraph provides instructions for removing and replacing the 371XXA Front Panel assembly.

Equipment Required:

- ❑ Open-end wrench, 1 in.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove handle assembles and all covers (paragraph 8-3).

Remove/Replace Procedure:

Step 1. Place the 371XXA in normal (top-side up) position.

Step 2. Remove the four corner screws and the top center screw that secure the front panel assembly to the chassis (see Figure 8-6).

Step 3. Place the 371XXA on its top (bottom-side up).

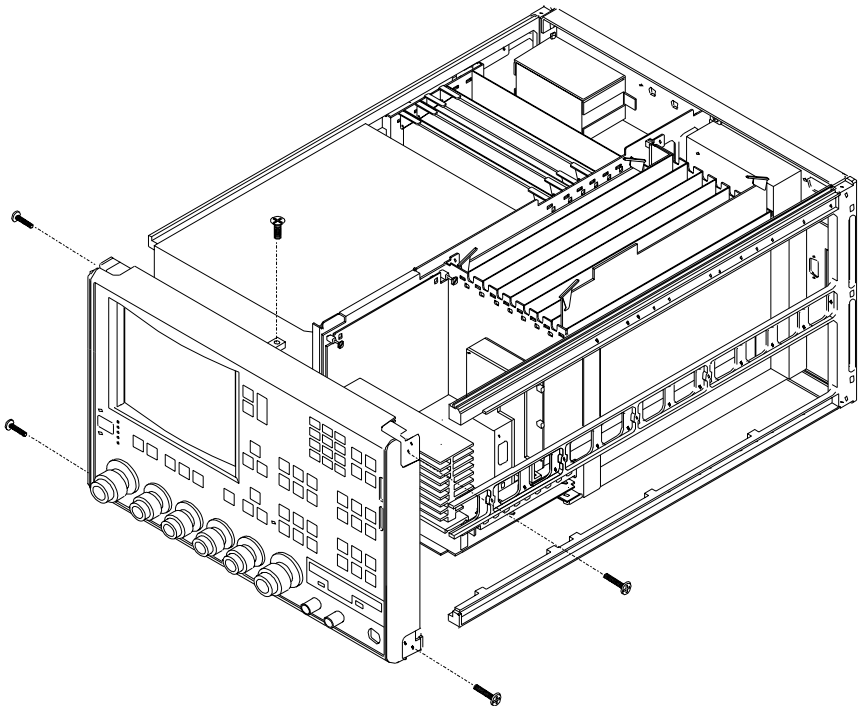


Figure 8-6. *Removal of Front Panel Assembly*

Step 4. Remove the screw that fastens the front panel casting extension lip to the Test Set Module tray. (See diagram at left.)

Step 5. Using a 1 in. open-end wrench, remove the nuts and washers that secure the Port 1 and Port 2 couplers/bridges to the front panel casting.

Step 6. Locate the cable from the front panel Power switch to connector J20 on the A17 Motherboard PCB. Disconnect at A17, J20 end.

Step 7. Locate the cable from the front panel Keyboard interface connector to connector J16 on the A17 Motherboard PCB. Disconnect at A17, J16 end.

Step 8. Locate the cables from the front panel Bias Input BNC connectors to connector P2 on the A18 Rear Panel PCB. Disconnect at A18, P2 end. (A18, P2 is the connector nearest to the bottom lip of the rear panel.)

Step 9. Gently pull front panel assembly several inches away from chassis. Locate cable from A17 Motherboard PCB to connector J1 on A20 Front Panel PCB. Disconnect at A20, J1 end.

Step 10. Separate the bias input cables (Step 8) from the cable harnesses, as necessary for removal. Pull front panel assembly free and set aside.

To replace the front panel assembly, perform the steps above in the reverse order.

8-9 REMOVE / REPLACE VGA DISPLAY MONITOR

This paragraph provides instructions for removing and replacing the internal VGA Display Monitor assembly.

NOTE

It is not necessary to remove the front panel assembly to perform this procedure.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

Remove/Replace Procedure:

Step 1. Place the 371XXA on its right side (monitor down).

Step 2. At rear of monitor assembly, disconnect:

- The power cord (from the Power Supply Module)
- The data cable from motherboard CRT connector, J14
- The two cables from motherboard BRITE/DEGAUSS connector, J15.

NOTE
All the the cables mentioned above have keyed connectors.

Step 3. Remove the four screws that fasten the monitor assembly to the chassis (see Figure 8-7). Do **not** unfasten the screw with the blue plastic washer under the screw head.

Step 4. Gently move the monitor assembly to the rear and lift away from chassis, with cables still attached. Place on work surface next to unit.

To replace the Internal VGA Display Monitor assembly, perform the steps above in the reverse order.

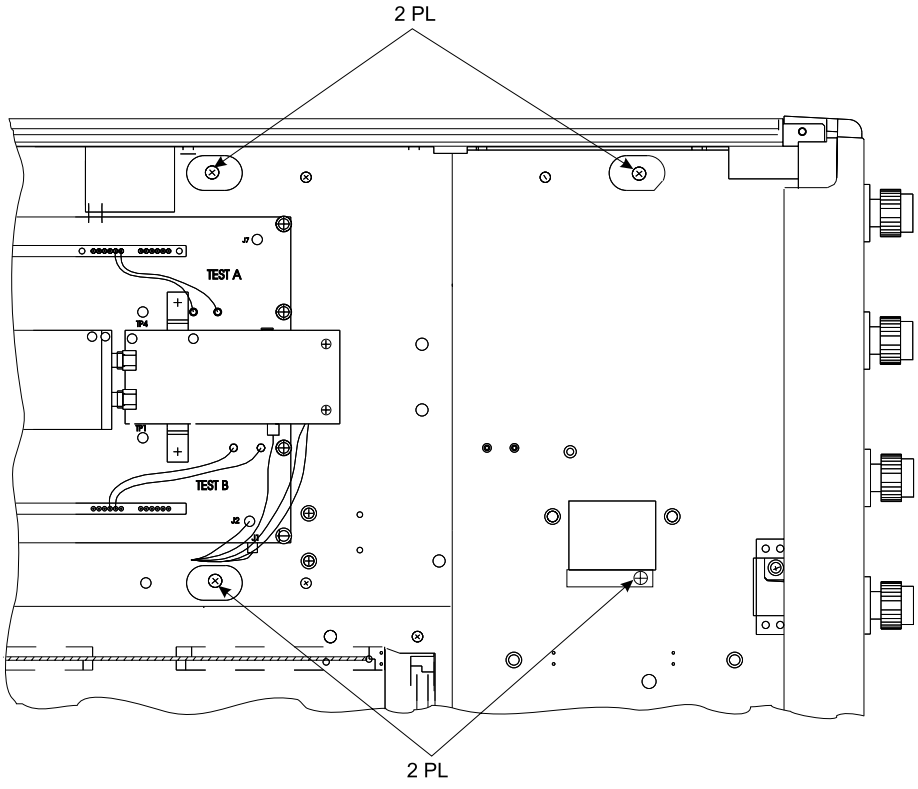


Figure 8-7. *Location of Internal VGA Monitor Assembly Mounting Screws*

8-10 REMOVE/REPLACE LCD BACKLIGHT LAMP

This paragraph provides instructions for the removal and replacement of the LCD Backlight Lamp, which is recommended at approximately 10,000 hours of operation, or if the display becomes dim.

NOTE
The front panel assembly does not have to be removed.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

Remove/Replace Procedure:

Step 1. Remove the LCD assembly (paragraph 8-10).

Step 2. Remove the Backlight Lamp cover as follows:

On Sharp LQ9D169 LCD displays, remove the three Phillips screws on the side opposite the PCB, then lift off the cover.

On Sharp LQ9D340 LCD displays, on the side opposite the PCB, remove the tape covering the center catch. Starting at one end, very carefully push each catch clear of its tab while gently lifting the cover. Release all five catches and remove the cover.

Step 3. Carefull replace the Backlight Lamp, while being careful not to apply pressure to the area where the glass tube and the end caps of the Backlight Lamp meet.

Step 4. Reinstall the Backlight Lamp cover.

Step 5. Reinstall the LCD Assembly and reconnect electrical connectors.

Step 6. Reinstall the top cover.

Step 7. Turn the instrument on. Adjust the Brightness Potentiometer at the rear panel for maximum display brightness.

8-11 REMOVE / REPLACE FLOPPY DISK DRIVE

This paragraph provides instructions for removing and replacing the Floppy Disk Drive assembly.

NOTE
It is not necessary to remove the front panel assembly to perform this procedure.

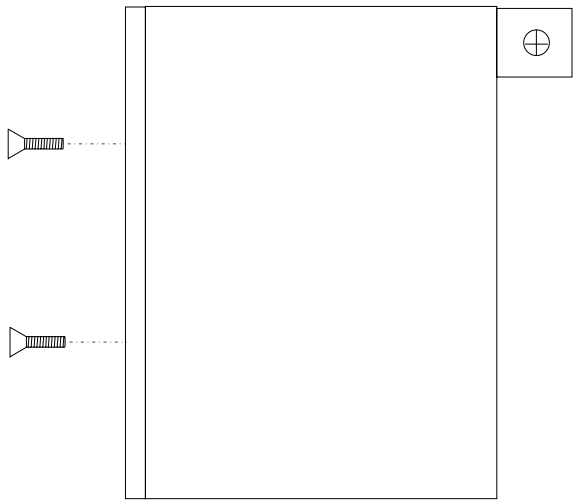


Figure 8-8. *Location of Floppy Disk Drive Assembly Mounting Plate Screws*

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

NOTE

All the the cables mentioned in the following procedure have "keyed" connectors.

Remove/Replace Procedure:

Step 1. Place the 371XXA on its top (bottom-side up).

Step 2. At the floppy drive, disconnect the four-conductor Disk Power cable that connects to J1 of the motherboard PCB.

Step 3. At J2 on the motherboard PCB, disconnect the Floppy Control (ribbon) cable that goes to the floppy drive.

Step 4. Remove the three screws that fasten the floppy disk drive mounting plate to the chassis and to the Test Set Module tray (see Figure 8-8).

Step 5. Carefully pull the floppy disk drive assembly to the rear and up to remove assembly.

Step 6. Carefully remove the Floppy Control cable from the rear of the floppy drive. Set aside for re-use.

To replace the Floppy Disk Drive assembly, perform the steps above in the reverse order.

8-12 REMOVE / REPLACE REAR PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the Rear Panel Assembly.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

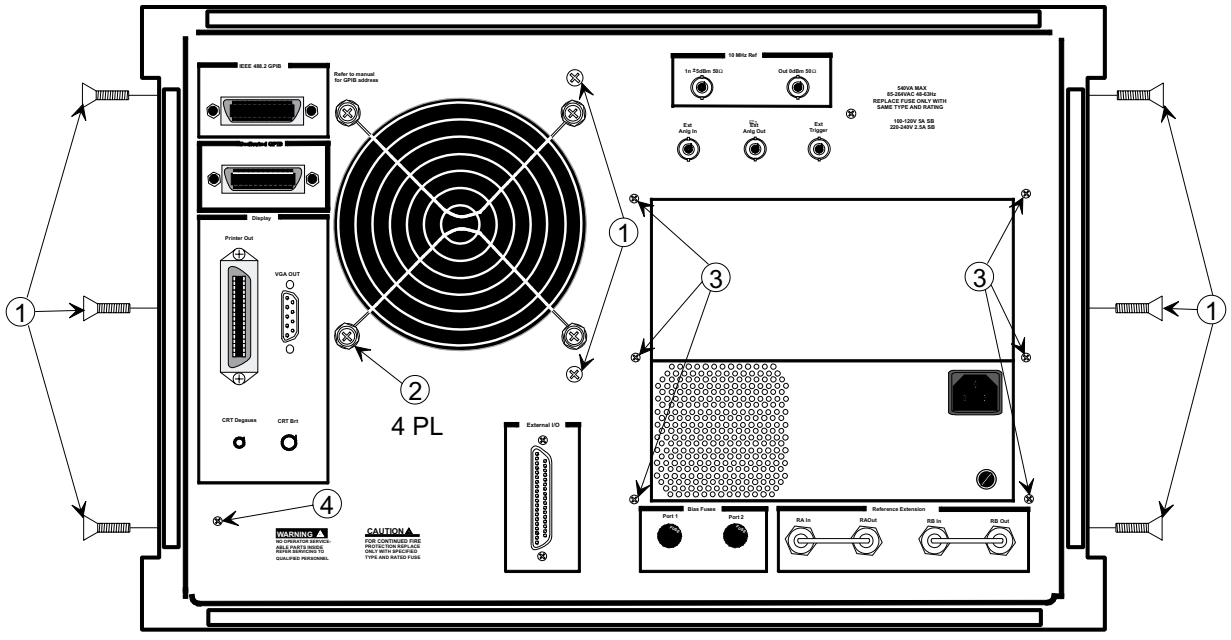
Remove/Replace Procedure:

Step 1. Place the 371XXA in normal (top-side up) position.

Step 2. Remove the three screws on each side of the chassis that fasten to the rear panel assembly. See Figure 8-9.

Step 3. Remove the two screws located near top and middle of rear panel (near fan-mounting screws). See Figure 8-9.

Step 4. Locate cable from the rear-panel 10 MHz Ref In BNC connector to connector J2 of A7 PCB. Disconnect at A7, J2 end. (Pull up gently to disconnect.)



①Rear Panel Asembly screws (par 8-11)
②Fan Assembly screws (par 8-12)
③Power Supply Assembly screws (par 8-13)
④A18 Rear Panel PCB screw (par 8-14)

Figure 8-9. *Location of Mounting Screws for Rear Panel Assemblies*

Step 5. Locate cable from the rear-panel 10 MHz Ref Out BNC connector to connector J3 of A7 PCB. Disconnect at A7, J3 end.

Step 6. Locate cable from the rear-panel Ext Anlg In BNC connector to connector J1 of A5 PCB. Disconnect at A5, J1 end.

Step 7. Place the 371XXA on its right side (monitor down).

Step 8. Locate the cables from the rear-panel Ext Trigger and Ext Anlg Out BNC connectors to connector P13 of the A18 Rear Panel PCB. Disconnect at A18, P13 end. (A18, P3 is the fourth connector away from the rear panel bottom lip.)

Step 9. Disconnect the large ribbon cable from connector P1 of the A18 PCB at motherboard connector J12.

Step 10. Disconnect the two cables from the Power Supply Module at motherboard connectors J4 and J13.

Step 11. Disconnect power cord from the Power Supply Module to the internal VGA Display Monitor at the display monitor.

Step 12. If 371XXA is equipped with Option 10, High Stability Time Base:

- Locate output cable from the high stability oscillator assembly (mounted above Power supply Module) to connector J1 of A7 PCB. Disconnect at A7, J1 end.
- Locate power cable from the high stability oscillator assembly to A17 Motherboard connector, J18. Disconnect at A17, J18 end.

Step 13. Place the 371XXA in normal (top-side up) position. Gently pull rear panel assembly away from chassis and lay flat on work surface. Remove cables from cable harnesses, as required.

To replace the Rear Panel Assembly, perform the steps above in the reverse order.

8-13 REMOVE / REPLACE FAN ASSEMBLY

This paragraph provides instructions for removing and replacing the Rear Panel Fan Assembly.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).
- ❑ Remove Rear Panel (paragraph 8-10).

Remove/Replace Procedure:

Step 1. Place the Rear Panel Assembly on the work surface with the A18 Rear Panel PCB up.

Step 2. Disconnect the two conductor fan power cable at connector P6 of the A18 PCB.

Step 3. Turn Rear Panel Assembly over, and remove the four screws that fasten the fan guard and fan assembly to the rear panel. See Figure 8-9.

Step 4. Remove the fan guard and separate the fan from the rear panel.

To replace the Rear Panel Fan Assembly, perform the steps above in the reverse order.

8-14 REMOVE / REPLACE POWER SUPPLY MODULE

This paragraph provides instructions for removing and replacing the Power Supply Module.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).
- ❑ Remove Rear Panel (paragraph 8-10).

Remove/Replace Procedure:

Step 1. Place the Rear Panel Assembly on the work surface with the Power Supply Module down.

Step 2. Remove the six screws from the rear panel that fasten it to the left and right edges of the Power Supply Module (see Figure 8-9). Gently separate the two units.

To replace the Power Supply Module, perform the steps above in the reverse order.

8-15 REMOVE / REPLACE A18 REAR PANEL PCB

This paragraph provides instructions for removing and replacing the A18 Rear Panel PCB assembly.

Equipment Required:

- ❑ Nut Driver, $\frac{9}{32}$ in.
- ❑ Nut Driver, $\frac{3}{16}$ in.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).
- ❑ Remove Rear Panel (paragraph 8-10).

Remove/Replace Procedure:

Step 1. Place the Rear Panel Assembly on the work surface with the A18 Rear Panel PCB up.

Step 2. Disconnect the two-conductor fan power cable at connector P6 of the A18 PCB.

Step 3. Disconnect the wiring for the rear panel Bias Fuses at connector P4 of the A18 PCB.

Step 4. Turn Rear Panel Assembly over. Remove screw located at lower left corner of the rear panel that fastens the A18 PCB to the Rear Panel Assembly (see Figure 8-9).

Step 5. Using a $\frac{9}{32}$ in. nut driver, remove the standoffs that fasten the IEEE 488.2 GPIB and Dedicated GPIB connectors to the rear panel.

Step 6. Using a $\frac{3}{16}$ in. nut driver, remove the standoffs that fasten the Printer Out, VGA Out, and External/IO connectors to the rear panel. Set standoffs aside for re-use.

Step 7. Carefully separate the A18 PCB from the rear panel.

To replace the A18 Rear Panel PCB assembly, perform the steps above in the reverse order.

8-16 REMOVE / REPLACE TEST SET MODULE ASSEMBLIES

The following paragraphs provide instructions for removing and replacing the RF/microwave components that comprise the Test Set Module .

Equipment Required:

- ❑ Connector torque wrench ($\frac{5}{16}$ in), WILTRON Model 01-201, or equivalent.
- ❑ Open-end wrench, 1 in.

CAUTION

Throughout these procedures, *always* use the $\frac{5}{16}$ in. connector torque wrench for connecting the Test Set Module semi-rigid coaxial lines and RF/microwave components. Use of improper tools may damage the connectors, resulting in degraded instrument performance.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

Power Amplifier

Use the following procedure to remove/replace the Power Amplifier assembly, which is common to all 371XXA models.

Procedure:

Step 1. Disconnect the Power Amplifier power cable at connector J5 of the A17 Motherboard PCB. Free the cable by separating it from the cable harness and by temporarily removing the A24 VME Terminator PCB.

Step 2. Disconnect the PWR AMP IN cable on the side of the Power Amplifier assembly; see Figure 8-12. (Pull out gently to disconnect.)

Step 3. Remove the two screws that fasten the Power Amplifier assembly to the test set tray. Remove the two screws that fastens the assembly feet to the Buffer Amplifier/Sampler assembly.

Step 4. Disconnect the Power Amplifier from the Buffer Amplifier/Sampler by carefully pulling up on the connector end of the rigid-coaxial line from the Power Amplifier. (See Figure 8-12.) Carefully lift the assembly from the Test Set Module.

To replace the Power Amplifier assembly, perform the steps above in the reverse order.

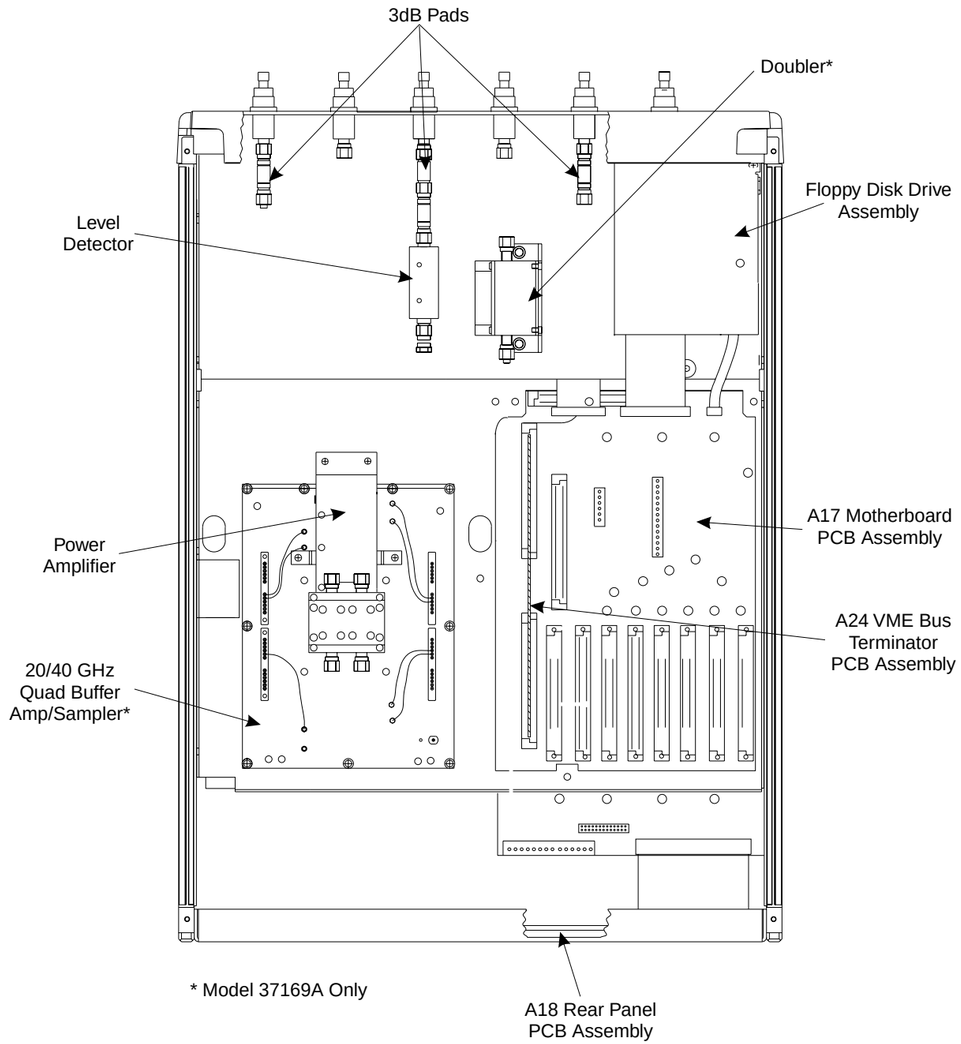
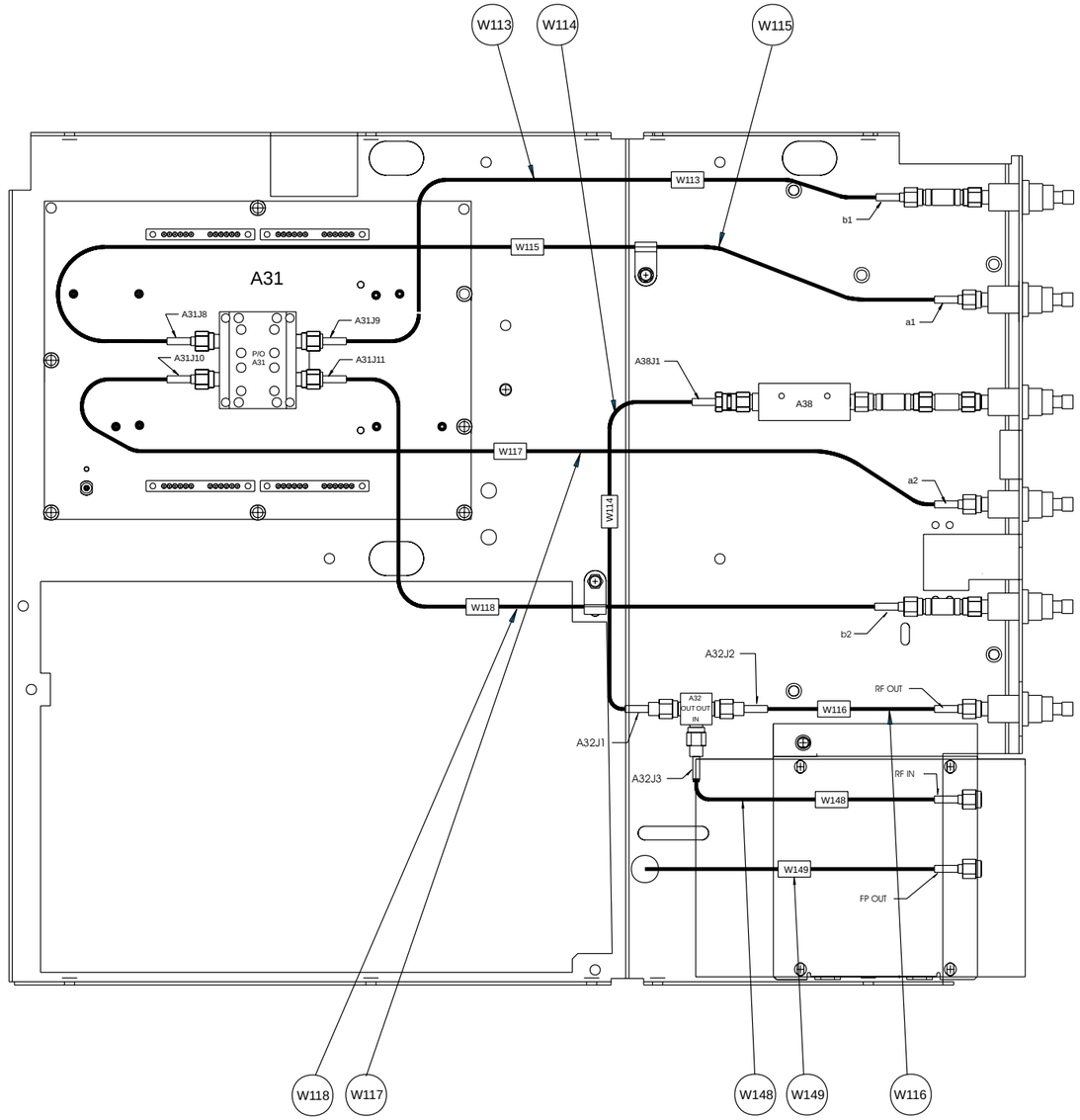


Figure 8-10. 371XX Module Components Layout Diagram



Note

This diagram shows cabling for the 37147A; cabling for the 37169A is similar, except that is contains a Doubler and corresponding cables.

Figure 8-11. 37147A Module Cabling Diagram

Buffer Amplifier/ Sampler(A31) Use the following procedure to remove/replace the Buffer Amplifier/ Sampler assemblies of all models.

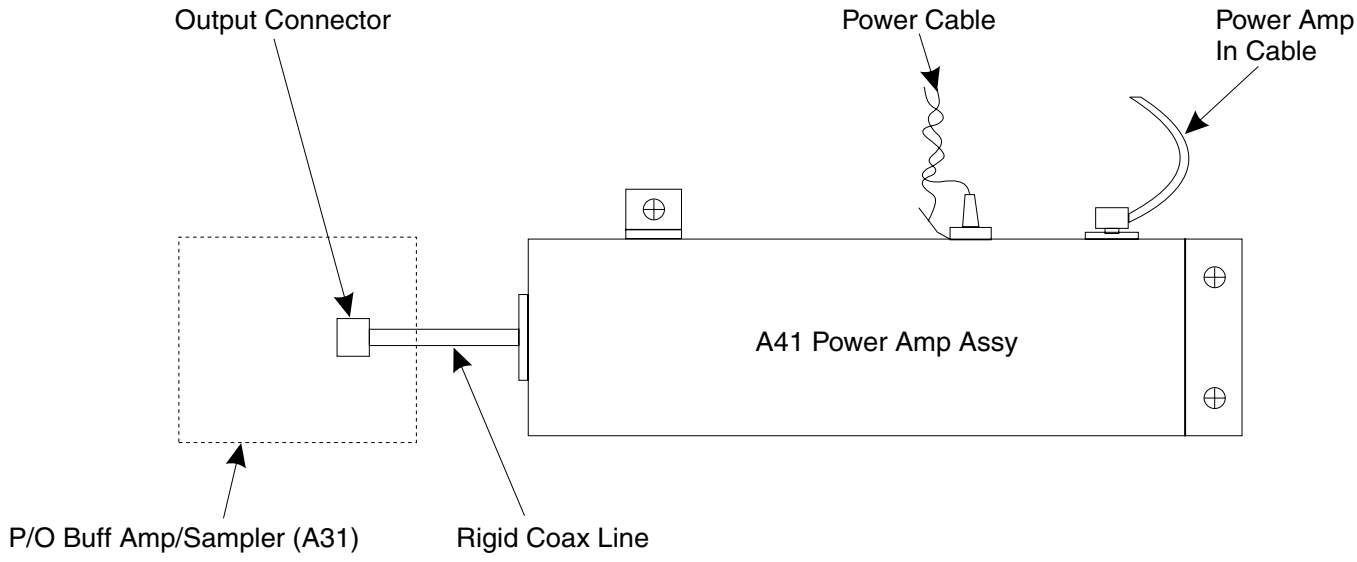


Figure 8-12. *A41 Power Amplifier Assembly, Details*

Preliminary:

❑ Remove the Power Amplifier assembly (see previous paragraph).

Procedure:

Step 1. Disconnect the semi-rigid coaxial lines, W83 and W84, from the 20 dB pads that are part of the Buffer Amplifier/Sampler assembly; see Figure 8-13. (For units with Option 11, the semi-rigid coaxial lines are W46 and W47.)

Step 2. Disconnect the cables from connectors J1 through J7 of the A31 Buffer Amplifier/Sampler assembly. (Pull up gently to disconnect.) Note that the connector end of each cable is marked with the associated A31 connector number.

Step 3. Disconnect the two cable connectors from the TEST A connector body on the Buffer Amplifier/Sampler assembly (see Figure 8-13). Similarly, disconnect the two cable connectors from the REF A connector body.NOTE

The matching pin numbers are identified on the cable connectors and on the connector body.)

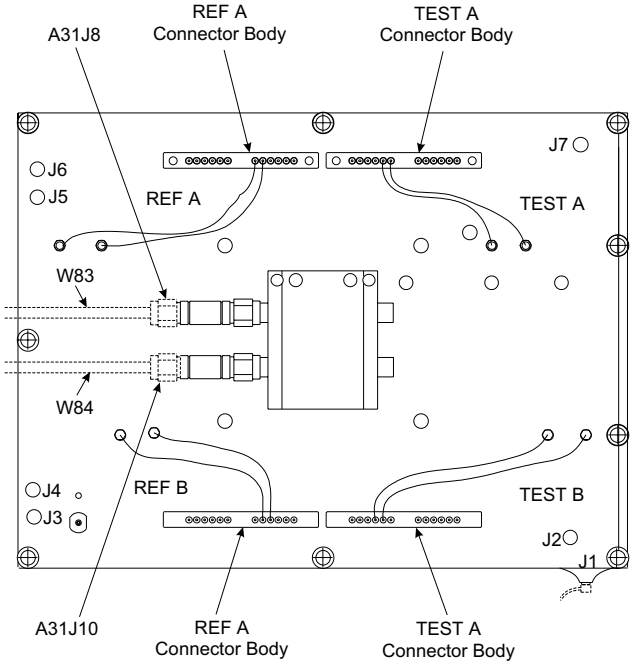


Figure 8-13. *A31 Buffer Amplifier/ Sampler Assembly, Details*

Step 4. Repeat Step 3 for the TEST B and REF B cable connectors.

Step 5. Remove the nine screws that fasten the Buffer Amplifier/Sampler assembly to the test set tray, and lift the assembly from the Test Set Module.

To replace the Buffer Amplifier/Sampler assembly, perform the steps above in the reverse order.

Switched Doubler Module Assembly

Use the following procedure to remove/replace the Switched Doubler Module (SDM) assembly for Model 37169A.

Procedure:

Step 1. Disconnect the SDM power cable from connector J17 of the A17 Motherboard PCB. Free cable from cable clip, as necessary.

Step 2. Disconnect the semi-rigid coaxial line W81 from the input connector of the SDM; see Figure 8-11.

Step 3. Remove the two screws that fasten the SDM to the Test Set Module tray.

Step 4. Disconnect the semi-rigid coaxial line W80 from the output connector of the SDM; see Figure 8-11. Carefully lift the assembly from the Test Set Module.

To replace the Switched Doubler Module assembly, perform the steps above in the reverse order.

8-17 REMOVE / REPLACE SIGNAL SOURCE MODULE ASSEMBLIES

The following paragraphs provide instructions for removing and replacing the RF/microwave components that comprise the Signal Source Module.

Equipment Required:

- ❑ Connector torque wrench ($\frac{5}{16}$ in), WILTRON Model 01-201, or equivalent.

CAUTION

Throughout these procedures, *always* use the $\frac{5}{16}$ in. connector torque wrench for connecting the Signal Source Module semi-rigid coaxial lines and rf/microwave components. Use of improper tools may damage the connectors, resulting in degraded instrument performance.

Preliminary:

- ❑ Switch 371XXA power **off**. Remove the power cord.
- ❑ Remove all covers (paragraph 8-3).

Removal of Signal Source Module

Use the following procedure to remove the Signal Source Module from the chassis. This step is necessary before any of the module components can be removed/replaced.

Procedure:

Step 1. Place the 371XXA on its top (bottom-side up).

Step 2. At J2 on the motherboard PCB, disconnect the Floppy Control (ribbon) cable that goes to the floppy drive. Dress the ribbon cable away from the Signal Source Module output connector; see Figure 8-10.

Step 3. Disconnect the semi-rigid coaxial line W87* from the output connector of the Signal Source Module.

Step 4. Place the 371XXA in normal (top-side up) position.

Step 5. Disconnect the cables from connectors J1 and J2 of the A21A2 Source Control PCB. (Pull up gently to disconnect.) Note that the connector end of each cable is marked with the associated A21A2 connector number.

Step 6. Disconnect the cable from connector J3** of the A21A2 Source Control PCB. Dress cables away from the Signal Source Module.

* W81 for Models 37169A

** Never operate unit with A21A2, J3 disconnected. Refer to Caution statement on

Step 7. Remove the three screws that fasten the Signal Source Module to the chassis side rail. See Figure 8-14.

Step 8. Loosen the two captive screws that fasten the Signal Source Module to the chassis (Figure 8-14).

Step 9. Pull up at the rear of the Signal Source Module to disconnect the A21A1 Source YIG Bias Control PCB from the A17 Motherboard PCB. Lift the module from the chassis and place on work surface.

To replace the Signal Source Module, perform the steps above in the reverse order.

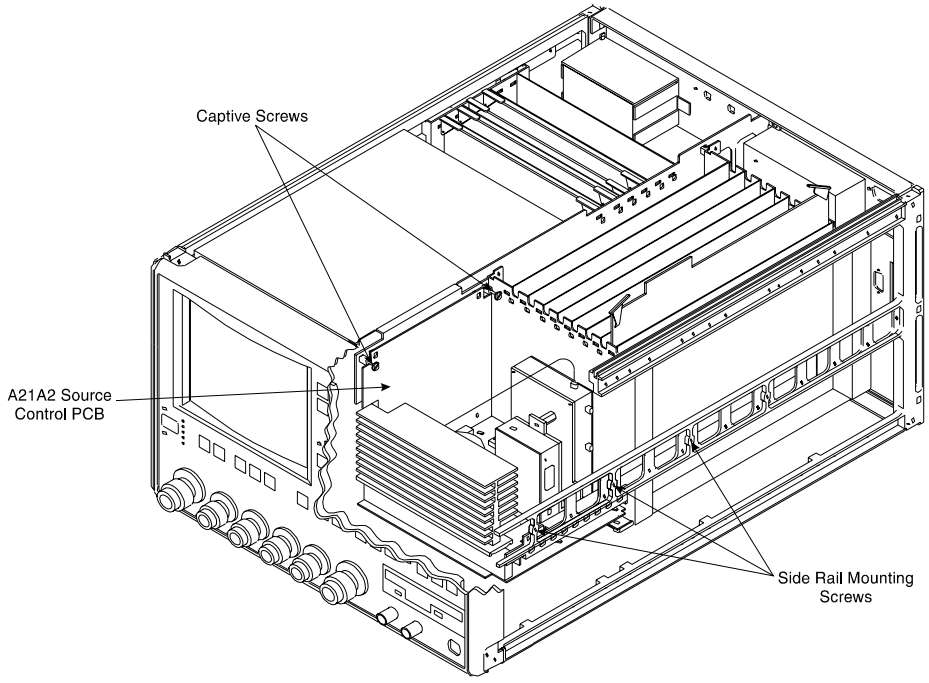


Figure 8-14. *Signal Source Module Removal Details*

A21A2 Source Control PCB Use the following procedure to remove/replace the A21A2 Source Control PCB assembly.

Procedure:

Step 1. Unfasten the two PCB retainers at the top corners of the A21A2 Source Control PCB (see Figure 8-15). To unfasten, turn screwdriver slot ¼ turn *counter-clockwise*.

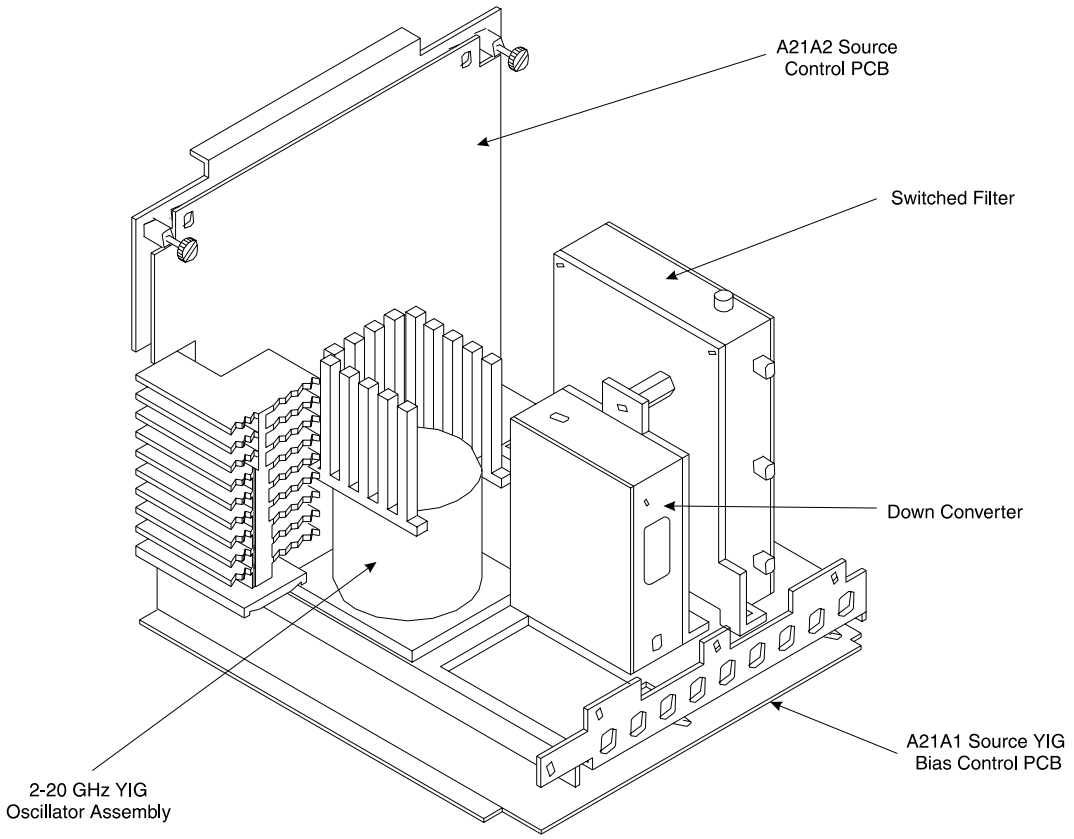


Figure 8-15. *Signal Source Module Assemblies Removal Details*

Step 2. Pull the top of the A21A2 PCB away from the source module chassis back plate to clear PCB retainers. Gently pull up to disconnect the A21A2 PCB from the socket on the A21A1 Source YIG Bias Control PC. Remove from Source Module.

To replace the A21A2 Source Control PCB assembly, perform the steps above in the reverse order.

A21A1 Source YIG Bias Control PCB

Use the following procedure to remove/replace the A21A1 Source YIG Bias Control PCB assembly.

Procedure:

Step 1. Disconnect the Switched Filter assembly power cable from connector J1 of the A21A1 Source YIG Bias Control PCB. (Pull up gently on ribbon cable to disconnect.)

Step 2. Similarly, disconnect the Down Converter assembly power cable from connector J4 of the A21A1 PCB.

Step 3. Disconnect the YIG Oscillator assembly power cable from connector J3 of the A21A1 PCB. Pull up on the flexible circuit connector "handle" to disconnect.

Step 4. Remove the screw that fastens the front apron of the source module chassis to the heatsink of the A21A1 PCB. See Figure 8-15.

Step 5. Remove the four screws that fastens the back plate of the source module chassis to the heatsink of the A21A1 PCB.

Step 6. Place the Signal Source Module on its' back plate.

Step 7. Unfasten the six PCB retainers on the bottom of the A21A1 PCB. (To unfasten, turn screwdriver slot ¼ turn *counter-clockwise*.) Gently separate the A21A1 PCB (including the heat sink) from the Signal Source Module.

To replace the A21A1 Source YIG Bias Control PCB assembly, perform the steps above in the reverse order.

Switched Filter Assembly

Use the following procedure to remove/replace the Switched Filter assembly.

Procedure:

Step 1. Disconnect the power cable from connector P1 at the rear of the Switched Filter assembly. (Use a small screw driver to pry up gently at each end of the connector, as necessary.)

Step 2. Disconnect the semi-rigid coaxial lines from connector J6 (top) and connector J3 (lower-front) of the Switched Filter assembly.

Step 3. Disconnect the semi-rigid coaxial line from the RF INPUT (top) connector of the *Down Converter* assembly.

Step 4. Remove the two screws that fasten the Switched Filter assembly to the source module chassis and lift the assembly from the Signal Source Module.

Step 5. Disconnect the semi-rigid coaxial line from connector J1 (bottom) of the Switched Filter assembly. Put this coaxial line aside for re-use.

NOTE

When replacing the Switched Filter assembly, connect the semi-rigid coaxial line to the bottom connector (J1), before attaching the assembly to the Signal Source Module.

To replace the Switched Filter assembly, perform the steps above in the reverse order.

Down Converter Assembly

Use the following procedure to remove/replace the Down Converter assembly.

Procedure:

Step 1. Disconnect the power cable from connector P1 at the front of the Down Converter assembly.

Step 2. Disconnect the semi-rigid coaxial lines from the RF INPUT connector and RF OUTPUT connector of the Down Converter assembly.

Step 3. Remove the two screws that fasten the Down Converter assembly to the source module chassis and lift the assembly from the Signal Source Module.

To replace the Down Converter assembly, perform the steps above in the reverse order.

YIG Oscillator Assembly

Use the following procedure to remove/replace the YIG Oscillator assembly.

Procedure:

Step 1. Disconnect the YIG Oscillator assembly power cable from connector J3 of the A21A1 PCB. Pull up on the flexible circuit connector “handle” to disconnect.

Step 2. Disconnect the semi-rigid coaxial line from the connector J6 (top) of the *Switched Filter* assembly.

Step 3. Remove the four screws that fasten the YIG Oscillator assembly to the source module chassis and lift the assembly from the Signal Source Module.

Step 4. Disconnect the semi-rigid coaxial line from the output connector of the YIG Oscillator assembly. Put this coaxial line aside for re-use.

NOTE

When replacing the YIG Oscillator assembly, connect the semi-rigid coaxial line removed in Step 4 to the output connector of the YIG Oscillator before attaching it to the Signal Source Module.

To replace the YIG Oscillator assembly, perform the steps above in the reverse order.

Appendix A
Diagnostics Menus

Table of Contents

Appendix A
Diagnostics Menus

A-1 INTRODUCTION

This appendix contains descriptions and usage information for the 371XXA Diagnostic Menus that are available via the front panel Option Menu key.

A-2 DIAGNOSTICS MENUS

The internal diagnostic capabilities of the 371XXA are accessed via the Options Menu key, which is part of the front panel Enhancement key group. The selections available from the top level DIAGNOSTICS menu (DG1) are listed below. See Figure A-1.

- Start Self Test
- Read Service Log
- Installed Options
- Peripheral Tests
- Troubleshooting
- H/W Calibrations

Start Self Test

The **START SELF TEST** selection, when invoked, will automatically test circuits throughout the 371XXA. Once invoked, it requires no external devices or interaction by the user. The net pass/fail result of the self-test is written to the CRT screen. Any self test failures will cause detailed failure information to be written into the service log.

This menu is available to service and non-service personnel.

Read Service Log

The **READ SERVICE LOG** menu allows for viewing, printing, clearing, and saving the internal system service log to floppy disk. The **CLEAR LOG** function is not recommended for non-service personnel.

The Service Log is made up of two parts, the log header and the error listing. The log header contains key system parameters such as initial system turn-on date/time/temperature, current power-on date/time/temperature, total operational hours, system model, serial, and installed option numbers, date/time/temperature stamp of current service log viewing session, date/time/temperature of internal hardware calibrations, and statistics about various internal system phase locking activities.

The error listing is a time ordered log containing the system faults with details about the system condition at the time of the fault.

NOTE

The service log must always be printed out or saved to disk and sent to the factory along with a failed assembly. Due to the importance of the information provided by the service log to ANRITSU factory Service Engineers, the exchange prices are only valid if the service log data (disk or printout) is submitted to the factory with the failed assembly.

This menu is available to service and non-service personnel. However, the service log should be cleared by service personnel only.

Installed Options The INSTALLED OPTIONS menu lists installed option numbers and descriptions.

This menu is available to service and non-service personnel.

Peripheral Tests The PERIPHERAL TESTS menu (DG3) tests the printer and GPIB ports, internal VGA monitor, front panel operation, and the external IBM compatible keyboard (if keyboard is connected). These tests will require some interaction and external devices such as the Printer Test Connector (ANRITSU PN: B39553), a GPIB cable, and an external IBM compatible keyboard as appropriate for the specific test.

This menu is available to service and non-service personnel.

Troubleshooting The TROUBLESHOOTING menu (DG4) and its sub-menus provide a host of pre-defined internal system modes and sub-system monitors that provide information useful in evaluating proper system operation. Most of these modes do not require any interaction or external test fixtures. (An exception is the **FIRST IF BANDPASS** selection which requires a thru line to be connected between the test ports.)

Menu DG4A and its sub-menus provide low level access to internal system hardware. These menus allow the user to control system latches, switches, and DACs. They also allow selection of key system states such as **set-on** or **search for lock**. Many internal analog voltages may be monitored via the 371XXA built-in DVM monitor network.

CAUTION

Always exit the troubleshooting mode via the DG4 menu selection **FINISHED, RECOVER FROM TROUBLESHOOTING** to insure proper system state recovery from your troubleshooting activities.

These menus are for service personnel only.

H/W Calibrations

The H/W CALIBRATIONS menus perform various internal automated hardware calibrations, including ALC and Frequency calibrations. The following equipment is required for these tests:

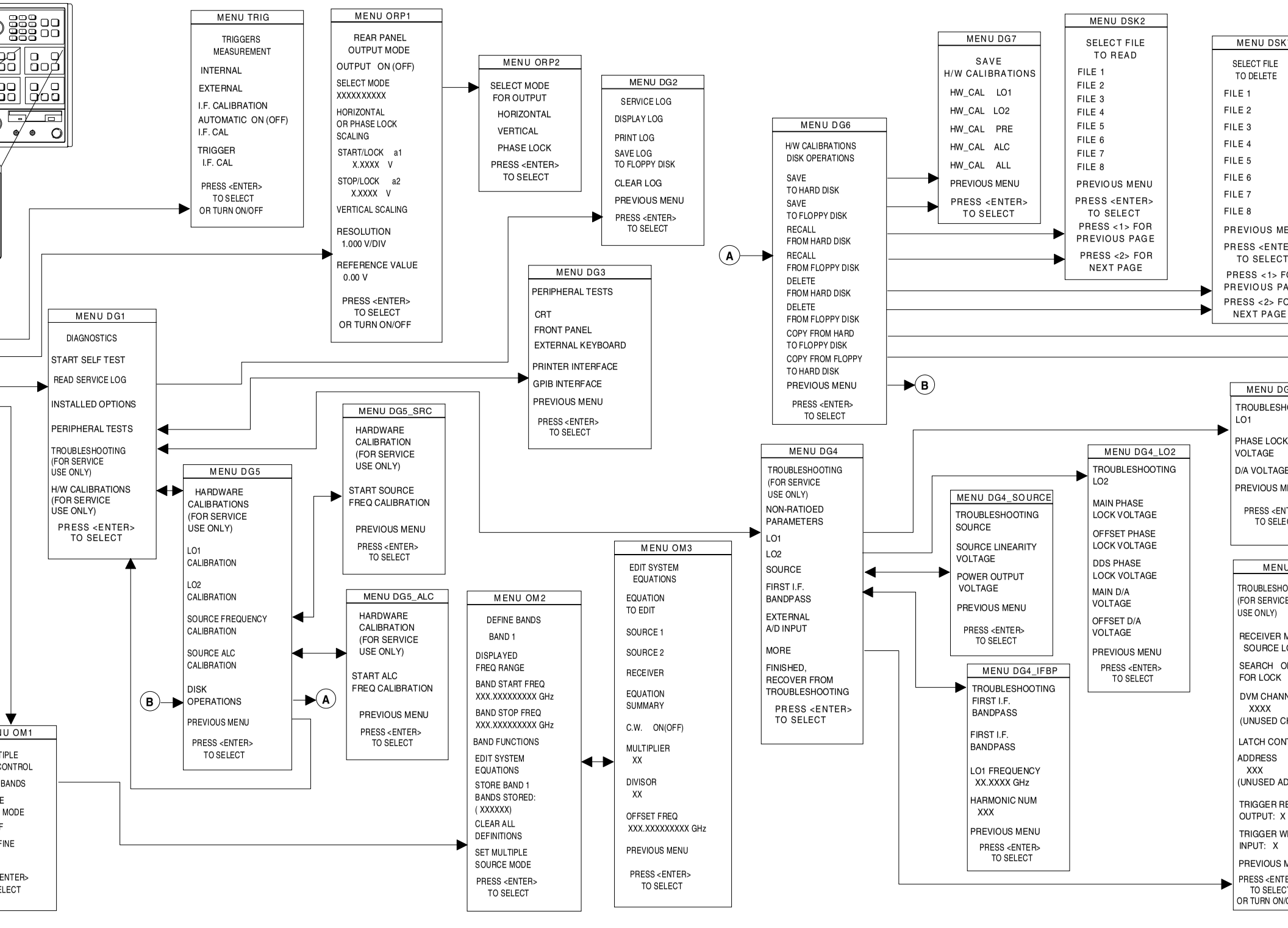
- Anritsu ML24XX Power Meter (or Gigatronics 8541/42 Power Meter)
- EIP 20 GHz series counter w/ GPIB (Option -08)

You need only connect the power meter or counter appropriate for the 371XXA model, invoke the calibration desired, and wait until complete. The ALC and Frequency calibrations take 5 to 10 minutes each. See Chapter 6, Adjustments, for further information.

The disk operations allow storage and retrieval of internal hardware calibration data to and from floppy disk. This feature will be useful when replacing the A9 Processor PCB since it contains the Battery Backed RAM where the internal hardware calibration data resides.

Automated field calibrations for the LO1 and LO2 assemblies are not presently implemented. Should these assemblies fail or require any adjustment, they must be replaced under the exchange assembly program (refer to Chapter 1).

These menus are for service personnel only.


MENU TRIG
TRIGGERS MEASUREMENT
INTERNAL
EXTERNAL
I.F. CALIBRATION
AUTOMATIC ON (OFF)
I.F. CAL
TRIGGER I.F. CAL
PRESS <ENTER> TO SELECT OR TURN ON/OFF
MENU ORP1
REAR PANEL OUTPUT MODE
OUTPUT ON (OFF)
SELECT MODE XXXXXXXXXX
HORIZONTAL OR PHASE LOCK SCALING
START/LOCK a1 X.XXXX V
STOP/LOCK a2 X.XXXX V
VERTICAL SCALING
RESOLUTION 1.000 V/DIV
REFERENCE VALUE 0.00 V
PRESS <ENTER> TO SELECT OR TURN ON/OFF
MENU ORP2
SELECT MODE FOR OUTPUT
HORIZONTAL
VERTICAL
PHASE LOCK
PRESS <ENTER> TO SELECT
MENU DG2
SERVICE LOG
DISPLAY LOG
PRINT LOG
SAVE LOG TO FLOPPY DISK
CLEAR LOG
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DG7
SAVE H/W CALIBRATIONS
HW_CAL LO1
HW_CAL LO2
HW_CAL PRE
HW_CAL ALC
HW_CAL ALL
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DSK2
SELECT FILE TO READ
FILE 1
FILE 2
FILE 3
FILE 4
FILE 5
FILE 6
FILE 7
FILE 8
PREVIOUS MENU
PRESS <ENTER> TO SELECT
PRESS <1> FOR PREVIOUS PAGE
PRESS <2> FOR NEXT PAGE
MENU DSK
SELECT FILE TO DELETE
FILE 1
FILE 2
FILE 3
FILE 4
FILE 5
FILE 6
FILE 7
FILE 8
PREVIOUS ME
PRESS <ENTE TO SELECT
PRESS <1> FO PREVIOUS PA
PRESS <2> FO NEXT PAGE
MENU DG6
H/W CALIBRATIONS DISK OPERATIONS
SAVE TO HARD DISK
SAVE TO FLOPPY DISK
RECALL FROM HARD DISK
RECALL FROM FLOPPY DISK
DELETE FROM HARD DISK
DELETE FROM FLOPPY DISK
COPY FROM HARD TO FLOPPY DISK
COPY FROM FLOPPY TO HARD DISK
PREVIOUS MENU
PRESS <ENTER> TO SELECT
A
B
MENU DG1
DIAGNOSTICS
START SELF TEST
READ SERVICE LOG
INSTALLED OPTIONS
PERIPHERAL TESTS
TROUBLESHOOTING (FOR SERVICE USE ONLY)
H/W CALIBRATIONS (FOR SERVICE USE ONLY)
PRESS <ENTER> TO SELECT
MENU DG3
PERIPHERAL TESTS
CRT
FRONT PANEL
EXTERNAL KEYBOARD
PRINTER INTERFACE
GPIB INTERFACE
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DG5_SRC
HARDWARE CALIBRATION (FOR SERVICE USE ONLY)
START SOURCE FREQ CALIBRATION
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DG5
HARDWARE CALIBRATIONS (FOR SERVICE USE ONLY)
LO1 CALIBRATION
LO2 CALIBRATION
SOURCE FREQUENCY CALIBRATION
SOURCE ALC CALIBRATION
DISK OPERATIONS
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DG5_ALC
HARDWARE CALIBRATION (FOR SERVICE USE ONLY)
START ALC FREQ CALIBRATION
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU OM2
DEFINE BANDS
BAND 1
DISPLAYED FREQ RANGE
BAND START FREQ XXX.XXXXXXXXX GHz
BAND STOP FREQ XXX.XXXXXXXXX GHz
BAND FUNCTIONS
EDIT SYSTEM EQUATIONS
STORE BAND 1 BANDS STORED: (XXXXXX)
CLEAR ALL DEFINITIONS
SET MULTIPLE SOURCE MODE
PRESS <ENTER> TO SELECT
MENU OM3
EDIT SYSTEM EQUATIONS
EQUATION TO EDIT
SOURCE 1
SOURCE 2
RECEIVER
EQUATION SUMMARY
C.W. ON(OFF)
MULTIPLIER XX
DIVISOR XX
OFFSET FREQ XXX.XXXXXXXXX GHz
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DG4
TROUBLESHOOTING (FOR SERVICE USE ONLY)
NON-RATIOED PARAMETERS
LO1
LO2
SOURCE
FIRST I.F. BANDPASS
EXTERNAL A/D INPUT
MORE
FINISHED, RECOVER FROM TROUBLESHOOTING
PRESS <ENTER> TO SELECT
MENU DG4_SOURCE
TROUBLESHOOTING SOURCE
SOURCE LINEARITY VOLTAGE
POWER OUTPUT VOLTAGE
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DG4_IFBP
TROUBLESHOOTING FIRST I.F. BANDPASS
FIRST I.F. BANDPASS
LO1 FREQUENCY XX.XXXX GHz
HARMONIC NUM XXX
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DG4_LO2
TROUBLESHOOTING LO2
MAIN PHASE LOCK VOLTAGE
OFFSET PHASE LOCK VOLTAGE
DDS PHASE LOCK VOLTAGE
MAIN D/A VOLTAGE
OFFSET D/A VOLTAGE
PREVIOUS MENU
PRESS <ENTER> TO SELECT
MENU DG
TROUBLESHO LO1
PHASE LOCK VOLTAGE
D/A VOLTAGE
PREVIOUS M
PRESS <EN TO SELE
MENU
TROUBLESHO (FOR SERVICE USE ONLY)
RECEIVER M SOURCE LO
SEARCH O FOR LOCK
DVM CHANN XXXX (UNUSED CH
LATCH CONT
ADDRESS XXX (UNUSED AD
TRIGGER RE OUTPUT: X
TRIGGER WI INPUT: X
PREVIOUS M
PRESS <ENTE TO SELEC OR TURN ON/O
U OM1
TIPLE CONTROL
BANDS
E MODE
F
FINE
ENTER>
ELECT

Appendix B
Error Messages

Table of Contents

Appendix
Error Messages

B-1 INTRODUCTION

This appendix provides a listing of error messages that appear on the 371XXA display or that are written to the internal software Service Log.

B-2 OPERATIONAL ERROR MESSAGES

Table B-1 provides a listing and description of the operational error messages. For the most part, these errors are displayed only on the 371XXA display and are caused by incorrectly operating the 371XXA.

B-3 DISK RELATED ERROR MESSAGES

Table B-2 provides a listing and description of the disk-related-error messages. The numbered errors in this group are also written to the Service Log, since they may indicate system problems.

B-4 GPIB RELATED ERROR MESSAGES

Table B-3 provides a listing and description of GPIB-related error messages. These errors are entered in the Service Log and output as part of the response of OGE/OGL commands.

B-5 SERVICE LOG ERROR MESSAGES

Table B-4 provides a listing of the error messages that are written to the internal system service log. Some of these messages may occur as a result of incorrectly programming the 371XXA. This includes the GPIB errors, 7204–7207, and errors in the 5000 range, RF Power. The RF Power errors may be triggered when setting the 371XXA power to a value greater than its reset level. This feature of the 371XXA lets you take advantage of all available power; however, accuracy cannot be guaranteed when power is unleveled. Refer to Chapter 5, paragraph 5-6 for additional guidance in interpreting these error codes.

The error messages in Table B-4 are numbered and organized as follows:

0000 - 0099 These messages generally indicate status or a pass/fail result of a Peripheral or Self test.

0100 - 3999 These messages primarily indicate a self-test failure with the suspect assembly number being the two high-order digits. For example, error 0111 indicates test 11 for the A1 assembly has failed, similarly, error 0814 is related to the A8 assembly test #14, and error 2138 is related to the A21 assembly test #38.

Since these errors are primarily self-test errors, they do not get displayed but only get written to the service log. Any exceptions to this

rule will be an assembly error code between xx00 - xx09, where xx is the assembly that is suspected of failing during normal operation. For example, error 0500 is a run-time error related to the A5 A/D assembly.

4000 - 4999 These messages indicate internal H/W calibration problems.

5000 - 5999 These messages indicate run-time RF power problems.

6000 - 6999 These messages indicate run-time phase lock problems. A letter or sequence of letters following the error message depict the suspect assembly(ies) as follows:

- A = 10 MHz Reference
- B = LO1 unlocked
- C = LO2 unlocked
- D = Source unlocked
- E = IF lock signal level too low
- F = External synthesizer unlocked
- G = LO3 unlocked
- None = Unknown

7000 - 7999 These messages indicate a run-time digital section problem.

8000 - 8999 These messages indicate a run-time processing system problem.

Table B-1. *Operational Error Messages (1 of 2)*

Error Message	Description	Corrective Action
ATTENUATOR UNAVAILABLE	Option 6 Port 2 Test Step Attenuator is not installed.	Install Option 6 Step Attenuator,
DIFFERENT H/W SETUP. RECALL ABORTED	Model and/or options is (are) different from the recalled setup.	Reconfigure system to duplicate the hardware setup that was used to store the saved data.
DIFFERENT S/W VERSION, RECALL ABORTED	Saved state not compatible with software version or options.	Load compatible software (S/W) version and retry.
FREQUENCIES HAVE REACHED UPPER LIMIT	Frequencies being defined in Multiple Source mode have reached upper limits of Sources.	Redefine frequencies to not exceed limits of Sources.
MEMORY LOCATION CORRUPTED	Requested memory location is corrupted.	None. If problem reoccurs after storing a new setup, contact ANRITSU Customer Service.
NO BANDS ARE STORED	No frequency bands have been defined and stored.	Define and store frequency bands to turn on Multiple Source mode.
NO STORED MEMORY DATA	No data is stored in memory for display or trace math.	Store or re-save measurement data.
OPTION NOT INSTALLED	Selected an option that is not installed.	None.
OUT OF CAL RANGE	Entered values out of the selected calibration range.	Change calibration range or re-enter values that are within the current range.
OUT OF H/W RANGE	Entered value is out of the instrument's hardware range.	Re-enter values that are within range.
OUT OF RANGE	Entered value is out of range.	Re-enter values that are within range.
RECEIVER OUT OF RANGE BY EQUATION	Equation defined in Multiple Source mode places receiver frequency out of range when attempting to store band.	Redefine frequency.
SOURCE 1 OUT OF RANGE BY EQUATION	Equation defined in Multiple Source mode places Source 1 frequency out of range when attempting to store band.	Redefine frequency.
SOURCE 2 OUT OF RANGE BY EQUATION	Equation defined in Multiple Source mode places Source 2 frequency out of range when attempting to store band.	Redefine frequency.
STANDARD CAL NOT VALID FOR WAVEGUIDE	Cannot use the standard method when calibrating with waveguide.	Use the Offset Short method with waveguide.
START F FOLLOWS PREVIOUS STOP F	Start frequency of current band immediately follows stop frequency of previous band. Cannot be modified.	None.
START MUST BE LESS THAN STOP	Entered start frequency is greater than the stop frequency.	Re-enter frequency values such that the start frequency is lower than the stop frequency.
STEP IS TOO LARGE	Entered harmonic frequency extends the stop out of range.	Re-enter so that harmonic frequency is within range.

Table B-1. *Operational Error Messages (2 of 2)*

Error Message	Description	Corrective Action
STOP IS OVER RANGE	Entered value exceeds the instrument's stop frequency.	Re-enter stop frequency.
SYSTEM NOT CALIBRATED	371XXA is uncalibrated for the selected measurement values.	Perform a measurement calibration.
TOO FEW POINTS, 2 MINIMUM	Entered too few discrete fill points, 2 is minimum.	Re-enter data points.
TOO MANY POINTS, 1601 MAXIMUM	Entered too many discrete fill points, 1601 points are the maximum allowed.	Re-enter data points.
UNDEFINED DIVIDE BY ZERO	Denominator cannot be zero in equation.	Make denominator a value other than zero.
WINDOW TOO SMALL	Attempted to set time domain range smaller than allowed	Re-enter larger time range.
OUT OF WINDOW RANGE	Attempted to set time domain range larger than allowed	Re-enter values within allowed range.

Table B-2. *Disk-Related-Error Messages (1 of 1)*

Error Message	Description	Corrective Action
7140 GENERAL FLOPPY DRIVE FAIL	Invalid disk media or format.	Use 1.44 MB diskette and/or format in the 371XXA.
7142 FLOPPY DISK READ ERROR	Read error when accessing disk file.	Use 1.44 MB diskette and/or format in the 371XXA.
7143: FLOPPY DISK WRITE ERROR	Error in writing to disk file.	Use 1.44 MB diskette and/or format in the 371XXA.
7147 FLOPPY DISK UNAVAILABLE	Floppy disk is not available.	Install floppy diskette and/or check floppy disk drive.
7170: GENERAL HARD DISK FAIL	General error in accessing hard disk.	Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive.
7172: HARD DISK READ ERROR	Read error when accessing disk file.	Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive.
7173: HARD DISK WRITE ERROR	Error in writing to disk file.	Retry and if still fails, reformat the hard disk drive and/or check floppy disk drive.
7177: HARD DISK UNAVAILABLE	Hard disk is not available.	Install hard disk drive and/or check operation of hard disk.
8140: GENERAL DISK BUFFER ERROR	Out of RAM.	Press the System State, Default Program key, and retry. This will reset the 371XXA to the factory default state.
FILE NOT FOUND	Disk file not found.	None.
FLOPPY DISK HAS NO ROOM FOR FILE	Floppy diskette is full.	Delete files or install new diskette.
FLOPPY DISK NOT READY	Floppy disk is not ready (or not installed.).	Install diskette in floppy drive.
FLOPPY DISK WRITE PROTECTED	Write protect tab in place on floppy diskette.	Remove write-protect tab.
HARD DISK HAS NO ROOM FOR FILE, DELETE EXISTING FILES(S) TO CREATE SPACE	Hard disk is full.	Delete unneeded files.

Table B-3. *GPIB-Related Error Messages (1 of 8)*

Error Message	Description
These errors are entered in the Service Log and output as part of the response of OGE/OGL commands for GPIB commands. The list is subdivided into the type of GPIB error: 7204..., 7205..., 7206..., and 7207.	
	7204 GPIB COMMAND ERROR DESCRIPTIONS
Faulty program mnemonic syntax	Generated when the program mnemonic found was not one of the currently defined program mnemonics for the 371XXA.
Faulty suffix mnemonic syntax	Generated when the suffix mnemonic found was not one of the currently defined suffix mnemonics for the 371XXA.
Faulty mnemonic syntax	Generated when the mnemonic found was not one of the currently defined program or suffix mnemonics for the 371XXA.
Missing Program Message Separator	Generated when the required semicolon preceding the next program mnemonic was not found.
Expected NRf data	Generated when a mnemonic is used that requires a trailing NRf numeric data element. The data element was either missing or the first character of the data element was not one of the acceptable NRf characters.
NRf mantissa too long	The maximum allowable number of characters in the NRf numeric element mantissa is 255.
Exponent magnitude too large	The maximum allowable exponent magnitude in an NRf element is +/— 32000.
Faulty NRf syntax	Can be any number of syntactical errors such as more than one decimal point, inclusion of a decimal point in the exponent field, an invalid character imbedded in the numeric or no exponent value following the ‘E’.
Expected String Program Data	Generated when a mnemonic is used that requires a trailing string data element. The date element was either missing or no open quote character was found.
Missing close quote character	Generated when a mnemonic is used that requires a trailing string data element. The open quote character was found, but the close quote character was not.
Expected Arbitrary Block data	Generated when a mnemonic is used that requires a trailing arbitrary block data element and the trailing element was not an arbitrary block data element. Or in some cases, the arbitrary block was empty.
Faulty Arbitrary Block	Generated when a defined length arbitrary block data element is terminated early with an EOI or an indefinite length arbitrary block data element is not properly terminated.
Missing Program Data Separator	Two data elements of a program mnemonic that requires multiple program data elements, are not properly separated from each other by a comma.
GET received during PM reception	Generated when the GPIB Command ‘Group Execute Trigger’ is received during the reception of a program message but before its proper termination with the end message. The partial program message up to but not including the ‘Group Execute Trigger’ will be executed. Execution of the Group Execute Trigger and any subsequent program message elements received before the end message will be skipped.

Table B-3. *GPIB-Related Error Messages (2 of 8)*

Error Message	Description
	7205 GPIB EXECUTION ERROR DESCRIPTIONS
Not permitted in a DDT command sequence	When executing a defined device trigger command sequence, a forbidden command was detected.
Too much Arbitrary Block data	The arbitrary block supplied contained more data than was necessary for the currently defined 371XXA state. This can occur when graph types, start/stop frequencies or data points are changed.
Insufficient Arbitrary Block data	The arbitrary block supplied did not have enough data for the currently defined 371XXA state. This can occur when graph types, start/stop frequencies or data points are changed.
Invalid parameter for current graph type	An attempt was made to program a non-existent parameter for the current graph type. For instance, a Smith chart does not have a reference or reference line position (mnemonics OFF and REF).
Parameter out of range	An attempt was made to program an out of integer range value for a parameter. This error is detected by the GPIB MANAGER when converting and rounding to the appropriate integral size (signed/unsigned char/short or long).
Parameter value not permitted	A parameter value was not found in the list of permissible values for that parameter.
CW marker sweep not permitted in time domain	The mnemonics M1C, M2C, M3C, M4C, M5C and M6C are forbidden in time domain.
Parameter unavailable in frequency domain	The mnemonic ODV and OTV are forbidden in frequency domain.
Port 2 Test Attenuator (OPT 6) not installed	The mnemonic TA2 is forbidden when the attenuator is not installed.
Time Domain (OPT 2) not installed	An attempt was made to use one of the time domain mnemonics when the option is not installed.
Return to Local not permitted in Local Lockout	The mnemonic RTL failed due to being in the Local Lockout mode.
Calibration does not exist	An attempt was made to turn on flat power correction or vector error correction when the corresponding calibration does not exist.
Cal term not available	An attempt was made to get a calibration term which does not exist for the current calibration type.
Invalid cal term for calibration type	An attempt was made to program a calibration term which does not exist for the current calibration type.
Front panel setup not valid	An attempt was made to get a front panel setup that did not contain a correct/valid state.
Normalization data not valid	An attempt was made to reference normalization data when there was no normalization data currently stored.
Command sequence too long	An attempt was made to define a device trigger command sequence which had more than 255 characters.
Unable to display menu	An attempt was made to display a menu which could not be displayed for the current 371XXA state.

Table B-3. *GPIB-Related Error Messages (3 of 8)*

Error Message	Description
String too long	An attempt was made to enter a string for the following mnemonics which exceeded the specified maximum length. LTD, LID, LMS and LNM - maximum length is 15 characters. LOC - maximum length is 79 characters.
Must specify a calibration type first	In order to perform a calibration, the calibration type must be specified by the use of one of the Cxx mnemonics (i.e. C12, C8T, etc.) PRIOR to the issuance of the mnemonics CWC, TDC or BEG.
Parameter value unchanged	An attempt was made to change a start/stop frequency or number of data points to a value outside of the current calibrated range with correction turned on.
Parameter change not permitted	An attempt was made to perform an illegal state change or action based on the current 371XXA state. This includes attempting to store an undefined band definition. Or certain changes from the calibration state or the calibration define state when defining discrete frequencies.
Parameter value out of range Parameter out of hardware range	An attempt was made to set a parameter to a value outside of the permissible range of values for the parameter.
Standard cal method not valid for waveguide	In a waveguide type of calibration, the standard (OSL) cal method is forbidden.
Out of calibrated range	An attempt was made to change a parameter not permitted to be changed with correction on.
Start must be must be less than stop	An attempt was made to set a new start frequency, distance or time greater than or equal to the current stop frequency, distance or time. Or to set a new stop frequency, distance or time less than or equal to the current start frequency, distance or time.
Tune mode requires a 12 term calibration	Perform a 12 term calibration prior to turning on tune mode.
Current and cal frequencies different	The flat power calibration setup does not match the current setup.
Stored data is invalid	An attempt was made to reference normalized data when normalized data was invalid.
Parameter change not permitted on current state	An attempt was made to change a parameter while IF cal was active. It is not expected that this message will ever be seen. If you see this message, notify the factory.
Calibration may not be valid	An attempt was made to repeat the previous calibration when there was no record of a previous calibration.
Calibration does not exist	An attempt was made to turn on flat power correction or vector error correction when the corresponding calibration does not exist.
Current calibration is erased	When turning on Multiple Source Mode with vector error correction on, the calibration is destroyed. Not really an error. Message is issued as a warning.
Time Domain and CW mode not permitted	An attempt was made to turn on a time domain mode in CW. This is not permitted.
Not permitted in Time Domain	An attempt was made to select a group delay display or CW mode when in time domain mode or to select a dual overlay display with a frequency/time domain mismatch.
Time Domain not allowed	An attempt was made to turn on a time domain mode but the current 371XXA state does not permit it.

Table B-3. *GPIB-Related Error Messages (4 of 8)*

Error Message	Description
Permitted only in diagnostic mode	Must put the 371XXA into the diagnostics mode via the SDG command before using this mnemonic.
Graph types not appropriate for dual overlay	While in dual overlay mode, and attempt was made to change one of the active graph types to a type which conflicts with dual overlay, or to change one of the active channels into or out of time domain which sets up a dual overlay conflict. Or an attempt was made to select dual overlay mode when there would be a graph type conflict for a frequency/time domain conflict.
New Discrete Fill not allowed in current state	Cannot set up a new discrete fill definition while performing a calibration or when correction is turned on. Also cannot do this when group delay is the graph type on the active channel.
Low Pass mode requires a harmonic sweep	Perform a TD harmonic sweep calibration prior to using this mnemonic.
Receiver out of range by equation	Problems with the internal source, external source or receiver equations in multiple source mode.
New start less than previous stop	An attempt was made to set the start frequency for the new multiple source mode band definition to a frequency less than the stop frequency of the previous band.
Bad filename	The supplied filename was bad. The filename can have 8 characters maximum. No extensions. The filename must start with and alpha type character (A thru Z). After that the allowable characters are alpha, numeric (0 thru 9) and underscore (_).
Conflict with rotary knob	You should not be using the rotary knob and the GPIB at the same time.
Too many data points for external source	A 6700B series external source can handle 501 data points. A 68000 series external source can handle 999 data points.
Recalled setup corrupted Hardware mismatch in recalled setup Software mismatch in recalled setup	These are problems with the recalled setup.
Too many data points for Discrete Fill	The maximum number of data points in discrete fill is 1601.
Not enough data points for Discrete Fill	The minimum number or data points in discrete fill is 2.
Discrete Fill end frequency out of range	The number of points for discrete fill puts the end frequency out of range.
Step is too large	When setting up a time domain harmonic sweep, cannot get 2 data points because the start frequency is too high for the approximate stop frequency. In a group delay display, the delay aperture percent of sweep is less than one step size.
Range too small	An attempt was made to set a distance or time span value too small. This can also be done via inappropriate values for start and stop.
Start or stop out of range	An attempt was made to set a distance or time start or stop value out of range. This can also be done via inappropriate values for center and span.
No bands defined	An attempt was made to turn on multiple source mode with no band definitions.

Table B-3. *GPIB-Related Error Messages (5 of 8)*

Error Message	Description
Out of frequencies for new band definition Source out of range by equation External source out of range by equation	The current set of multiple source mode bands use up all the frequency range of the 371XXA. Therefore, no more bands can be defined.
File is read only	An attempt was made to write to a write protected file.
File not found	An attempt was made to access a non-existent file.
Floppy drive not ready	An attempt was made to access the floppy drive with no floppy disk installed.
Floppy disk full Hard disk full	An attempt was made to write to a floppy disk or the hard disk when no space was left on the disk.
Floppy disk write protected	An attempt was made to write to a write protected floppy disk.
Recalled setup or data file corrupt	An attempt to recall a setup from internal memory, the GPIB or disk failed due to software revision or hardware mismatch or checksum error.
New frequency list not allowed in current state	Cannot set up a new discrete fill definition while performing a calibration or when correction is turned on. Also, cannot do this when group delay is the graph type on the active channel.
State change not permitted	An attempt was made to perform an illegal state change or action based on the current instrument state. This includes attempting to store (1) an undefined band definition, (2) certain changes from the calibration state, or (3) the cal define state when defining discrete frequencies.
Faulty label or file name	The label or file name associated with the current mnemonic is faulty.
Illegal characters in filename	The first character in a filename must be an alpha type. The remaining characters can be alpha, numeric, or underscores. An extension is not permitted.
Filename too long	The maximum lendngth for filenames is 8 characters. An extension is not permitted.
Floppy disk read error Floppy disk write error Hard disk read error Hard disk write error	Read or write error(s) occurred while attempting to access the indicated disk.
Floppy disk not found Hard disk not found General disk buffer error General floppy drive failure Floppy disk init failure General hard disk failure Hard disk control failure Hard disk init failure Unknown disk error	Other error messages which suggest that the indicated drive is in need of service.

Table B-3. *GPIB-Related Error Messages (6 of 8)*

Error Message	Description
	7205 GPIB QUERY ERROR DESCRIPTIONS
No Response data available	Generated if the controller attempts to read response data from the 371XXA and none is available.
No Response data after PM completion	This is the same as the 'no response data available' case above except that a program message was currently being parsed and executed when the controller attempted to read data. Detection of this error was deferred until the parser/execution block was finished with the current program message and it was observed that no response data was generated.
Response after Indefinite Response discarded	This error is generated when the 371XXA's output queue has already received an Arbitrary ASCII response data element and an attempt is made to place another response data element of any kind into the queue. The new response data element is discarded.
Interrupted - Response data discarded	This error is detected when the output queue contains unread response data and the controller sends a new program message. The response data is discarded.
Unterminated - Partial PM will be executed	This error is detected when the 371XXA's input queue is currently receiving a program message but has not yet received the end message, and the controller attempts to read response data from the 371XXA. The partial program message in the input queue is executed as if it were properly terminated.
Deadlock - Response data discarded	This error is detected when both of the 371XXA's input and output queues are full and the controller attempts to send another data byte. In order to prevent bus deadlock, the contents of the output queue are discarded.
	7205 GPIB DEVICE DEPENDENT ERROR DESCRIPTIONS
Q_SEND failure in [a procedure name]	An unsuccessful attempt was made to send a message to a task. The procedure name is the place in the software where the error was detected.
Q_RECEIVE failure in [a procedure name]	A failure was detected while waiting for the reception of a message from a task. The procedure name is the place in the software where the error was detected.
Unable to allocate memory in [a procedure name]	An attempt was made to allocate some temporary memory in order to accomplish a task directed in the program message. The procedure name is the place in the software where the error was detected.

Table B-3. *GPIB-Related Error Messages (6 of 8)*

Error Message	Description
Unable to release memory in [a procedure name]	An attempt was made to return some temporary memory within a task and the return failed for some reason. The procedure name is the place in the software where the error was detected.
Unable to get service/error log	An unsuccessful attempt was made to get a copy of the service or error log.
Unable to get calibration term	An unsuccessful attempt was made to get a calibration term.
Unable to get raw or corrected data	An unsuccessful attempt was made to get raw or corrected data.
Unable to get final data	An unsuccessful attempt was made to get final data.
Unable to get setup or data	An unsuccessful attempt was made to get the frequency list from the database.
Unable to get setup	An unsuccessful attempt was made to get a front panel setup.
Unable to store setup	An unsuccessful attempt was made to save a front panel setup.
Unable to get frequency list	An unsuccessful attempt was made to get setup, trace, or tabular datat from the database.
Unable to store label	An unsuccessful attempt was made to store a label in the database.
Calibration step failure	An error occurred while waiting for completion of a data collection sequence in calibration.

Table B-4. *Service Log Error Messages (1 of 3)*

0000 INFORMATIONAL MESSAGE	0525 PWR SUPPLY -18V FAIL
0000 SELF TEST INFO MESSAGE	0526 PWR SUPPLY +27V FAIL
0094 PRNT INTERFACE TEST PASSED	0527 PWR SUPPLY -27V FAIL
0095 PRNT INTERFACE TEST FAILED	0611 TB IF COMM FAIL
0096 GPIB INTERFACE TEST PASSED	0612 TB IF 10V REF FAIL
0097 GPIB INTERFACE TEST FAILED	0613 TB IF LEVEL STATUS FAIL
0098 SELF TEST PASSED	0614 TB PHS CONTROL FAIL
0099 SELF TEST FAILED	0711 LO3 COMM FAIL
0111 LO1 COMM FAIL	0712 LO3 REF OSC FAIL
0112 LO1 PRE TUNE DAC FAIL	0713 LO3 48.4 LCK IND FAIL
0113 LO1 PHS LCK IND FAIL	0714 LO3 48.4 LCK ERR VOL FAIL
0114 PHS LCK ERR VOL OUT OF TOL	0715 LO3 CAL REF PHS FAIL
0115 LO1 LCK TIME FAIL	0811 SL SIG SEP COMM FAIL
0211 LO2 COMM FAIL	0812 DAC ADJUSTMENT FAIL
0212 LO2 MAIN PREST DAC FAIL	0813 TRANSFER SWITCH CNTRL FAIL
0213 LO2 OFFS PREST DAC FAIL	0814 SRC LCK POL CONTROL FAIL
0214 MAIN PHS LCK ERR VOL FAIL	0815 DIRECT MODE ATTEN FAIL
0215 OFFST PHS LCK ERR VOL FAIL	0911 A9 VME BUS INTERFACE FAIL
0216 DDS PHS LCK ERR VOL FAIL	0912 BBRAM CHECK FAIL
0217 MAIN PHS LCK IND FAIL	0913 SRAM CHECK FAIL
0218 OFFST PHS LCK IND FAIL	0914 SCSI DEVICE FAIL
0219 DDS PHS LCK IND FAIL	0915 MCCHIP FAIL
0220 LO2 LCK TIME FAIL	0915 MCCHIP TIMER 1 FAIL
0221 LO2 SRC TRACKING FAIL	0916 MCCHIP TIMER 2 FAIL
0311 TA IF COMM FAIL	0917 MCCHIP TIMER 3 FAIL
0312 TA IF 10V REF FAIL	0918 MCCHIP TIMER 4 FAIL
0313 TA IF LEVEL STATUS FAIL	0919 CLOCK NOT RUNNING
0314 TA PHS CONTROL FAIL	1311 A13 VME BUS INTERFACE FAIL
0411 REF IF COMM FAIL	1312 EXT KEYBD CNTRL FAIL
0412 REF IF 10V REF FAIL	1313 FLOPPY DISK CNTRL FAIL
0413 REF IF LEV STATUS FAIL	1411 A14 VME BUS INTERFACE FAIL
0414 REF PHS CONTROL FAIL	1511 A15 VME BUS INTERFACE FAIL
0500 A TO D CONVERSION FAIL	1512 VRAM CHECK FAIL
0511 A TO D COMM FAIL	1611 HARD DISK CONTROL FAIL
0512 A TO D 8 BIT D TO A FAIL	1811 AUXILLARY IO FAIL
0513 A TO D 12 BIT A TO D FAIL	1912 FRONT PANEL CNTRL FAIL
0514 A TO D STEERING DAC FAIL	1913 ROTARY KNOB FAIL
0515 A TO D CONV ACCURACY FAIL	2111 SRC COMM FAIL
0516 A TO D SAMPL HOLD FAIL	2112 SRC FTUNE DAC FAIL
0517 IF SYNC FAIL	2113 SRC STATE MACHINE DAC FAIL
0518 PWR SUPPLY SYNC FAIL	2114 SRC FM CAL FAIL
0519 A TO D EXT ANAL OUTP FAIL	2115 SRC F TUNE PATH BND1 FAIL
0520 PWR SUPPLY +5V FAIL	2116 SRC F TUNE PATH BND2 FAIL
0521 PWR SUPPLY +9V FAIL	2117 SRC F TUNE PATH BND3 FAIL
0522 PWR SUPPLY +12V FAIL	2118 SRC F TUNE PATH BND4 FAIL
0524 PWR SUPPLY +18V FAIL	2119 SRC F TUNE PATH BND5 FAIL

Table B-4. *Service Log Error Messages (2 of 3)*

2120 SRC F TUNE PATH BND6 FAIL	7177 HARD DISK UNAVAILABLE
2121 SRC F TUNE PATH BND7 FAIL	7199 HARD DISK INIT FAIL
2122 SRC F TUNE PATH BND8 FAIL	7200 IEEE 488.2 GPIB BUS ERROR
2123 SRC F TUNE PATH BND9 FAIL	7201 ABORTED MESSAGES
2124 SRC F TUNE PATH BND10 FAIL	7202 NOTHING TO SAY
2125 SRC PWR LEVEL DAC FAIL	7203 NO LISTENER ON BUS
2126 SRC DETECTOR ZERO CAL FAIL	7204 GPIB COMMAND ERROR
2127 SRC ALC CAL BND1 FAIL	7205 GPIB EXECUTION ERROR
2128 SRC ALC CAL BND2 FAIL	7206 GPIB DEVICE SPECIFIC ERROR
2129 SRC ALC CAL BND3 FAIL	7207 GPIB QUERY ERROR
2130 SRC ALC CAL BND4 FAIL	7210 DEDICATED GPIB BUS ERROR
2131 SRC ALC CAL BND5 FAIL	7220 PLOTTER NOT RESPONDING
2132 SRC ALC CAL BND6 FAIL	7221 PLOTTER NOT READY
2133 SRC ALC CAL BND7 FAIL	7222 PLOTTER OUT OF PAPER
2134 SRC ALC CAL BND8 FAIL	7223 PLOTTER PEN UP
2135 SRC ALC CAL BND9 FAIL	7230 POWER METER NOT RESPONDING
2136 SRC ALC CAL BND10 FAIL	7240 FRQ COUNTER NOT RESPONDING
2137 SRC A1 FM PATH TUNE FAIL	7250 EXT SOURCE NOT RESPONDING
2138 SRC A2 FM PATH TUNE FAIL	7310 PRINTER NOT RESPONDING
4100 LO1 CAL FAIL	7311 PRINTER NOT READY
4200 LO2 CAL FAIL	7312 PRINTER OUT OF PAPER
4301 SRC FREQ CAL MEAS UNSTABLE	7320 AUX I/O PORT ERROR
4302 SRC FREQ FM MAIN CAL FAIL	7330 SERIAL PORT ERROR
4303 SRC FREQ FM SENS CAL FAIL	7340 ETHERNET PORT ERROR
4304 SRC FREQ CAL VERIFY FAIL	7350 EXT TRIG RATE TOO FAST
4401 SRC ALC LOG AMP CAL FAIL	7410 EXT KYBD ERROR
4402 SRC ALC CAL VERIFY FAIL	8100 PWR FAIL
4500 IF CAL FAIL	8110 GENERAL VME BUS FAIL
4600 GAIN RANGING ERROR	8120 GENERAL MEMORY FAIL
4700 STATE MACHINE FAIL	8121 NON-VOLATILE MEMORY FAIL
5110 RF PWR UNLEVELED	8130 PROCESSING FAIL
5210 REF A CHAN RF OVERLOAD	8140 GENERAL DISK BUFFER ERR
5220 REF B CHAN RF OVERLOAD	SRC PWR CHANGED AFTER CAL
5230 TA CHAN RF OVERLOAD	ATTEN CHANGED AFTER CAL
5240 TB CHAN RF OVERLOAD	CAL DATE TOO OLD
6001 - 6128 PHASE LOCK FAILURE	CAL COEFF NOT INSTALLED
7100 FILE MARKED READ ONLY	TEMP TOO HIGH
7140 GENERAL FLOPPY DRIVE FAIL	TOO HIGH TEMP CHANGE
7142 FLOPPY DISK READ ERROR	H/W RETUNED SINCE CAL
7143 FLOPPY DISK WRITE ERROR	BAD FILENAME
7146 FLOPPY DISK CHANGED	CAL MAY BE INVALID
7147 FLOPPY DISK UNAVAILABLE	FLAT CAL MAY BE INVALID
7169 FLOPPY INIT FAIL	FLAT PWR TURNED OFF
7170 GENERAL HARD DISK FAIL	HARD COPY OUTPUT ABORTED
7172 HARD DISK READ ERROR	CORRECTION UNAVAILABLE
7173 HARD DISK WRITE ERROR	TIME DOMAIN INVALID

Table B-4. *Service Log Error Messages (3 of 3)*

GROUP DELAY INVALID	TRANS FREQ RESP BOTH PATHS CORR
GATE MUST BE ON	REFL ONLY PORT 1 CORRECTION
SMOOTHING INVALID	REFL ONLY PORT 2 CORRECTION
MEMORY DATA INVALID	REFL ONLY BOTH PORTS CORRECTION
NEED HARMONIC SWEEP	2 PORT FWD PATH CORRECTION
NON-LOCKED REF N/A	2 PORT REV PATH CORRECTION
PARAMETER INVALID	2 PORT FWD PATH REV DUT CORR
DATA DRAWING OFF	2 PORT REV PATH REV DUT CORR
STORED RF CORR CLEARED	12-TERM CORRECTION
STORED TRACE DATA CLEARED	DEFINING MULTIPLE SOURCE BANDS
STORED SRC FREQ CAL CLEARED	TS: LO1 VCO MAIN
STORED SRC ALC CAL CLEARED	TS: LO1 DAC MAIN
STORED INSTR STATE CLEARED	TS: LO2 VCO MAIN
INVALID MODEL NUMBER	TS: LO2 VCO OFFSET
ABORTED: H/W DIFFERENT	TS: LO2 VCO VDDS
ABORTED: S/W DIFFERENT	TS: LO2 DAC MAIN
CORRUPT OR INCOMPATIBLE FILE	TS: LO2 DAC OFFSET
NOT ALLOWED AT THIS TIME	TS: SOURCE LINEARITY
STORED SWP FREQS CLEARED	TS: SOURCE POWER
HARD COPY DATA CAPTURE FAILED	TS: FIRST IF BANDPASS
PRINTER BUSY	TS: EXTERNAL INPUT
STORED SERIAL NUMBER CLEARED	TS: NON-RATIOED PARAMETERS
END FRONT PANNEL ERRORS	TS: GENERIC TROUBLESHOOTING
WORKING...	WIPING OUT RESERVED PARAMETERS
CALIBRATING I.F. PLEASE WAIT	WIPING OUT FRONT PANEL MEMORIES
TRANS FREQ RESP FWD CORRECTION	SETTING SYSTEM DEFAULT VALUES
TRANS FREQ RESP REV CORRECTION	

Appendix C
Connector Maintenance Check Procedures

Table of Contents

Appendix C
Connector Maintenance Check Procedures

C-1 INTRODUCTION

This appendix provides general, precautionary information and instructions pertaining to precision connectors.

C-2 PRECAUTIONS

The following paragraphs are precautionary notes relating to maintenance considerations for precision connectors

Pin Depth Problems

Based on ANRITSU precision components returned for repair, destructive pin depth of mating connectors is the major cause of failure in the field. When a precision component is mated with a connector having a destructive pin depth, damage will likely occur to the precision component's connector. A connector is considered to have destructive pin depth when the center pin is too long in respect to the connector's reference plane (Figure C-1).

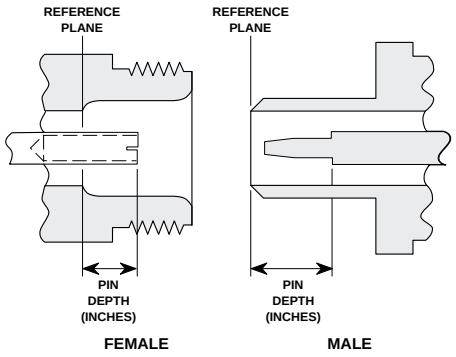


Figure C-1.

Before mating an unknown or new device with your 371XXA Port connectors or calibration devices, always measure the pin depth of the device's connectors. Use a ANRITSU Pin Depth Gauge, or equivalent, for these measurements (Figure C-2). Also, measure the connector pin-depth of a device when intermittent or degraded performance is suspected.

Gauging sets for measuring the pin-depth of precision connectors are available from your nearest ANRITSU Service center, or from the factory. Instructions for measuring connector pin-depth are included with the gauging set(s).

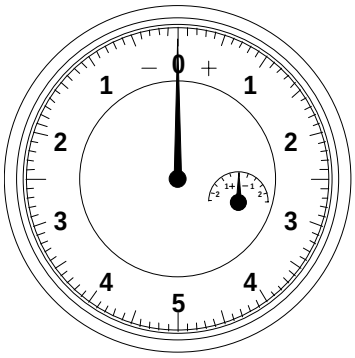


Figure C-2. *Pin Depth Gauge*

Pin-Depth Tolerance

The center pin of a precision connector has a tolerances measured in mils (one mil = 1/1000 inch). The connectors of test devices may not be precision types and they may not have the proper pin-depth. These connectors should be measured before mating to ensure suitability.

When gauging pin depth, if the connector being measured indicates out of tolerance in the "+" region of the gauge (Table C-1), the center pin is too long. *Mating under this condition will likely damage the mating connector.* On the other hand, if the test device connector indicates out of tolerance in the "–" region, the center pin is too short. While this will not cause any damage, it will result in a poor connection and a consequent degradation in performance.

Avoid Over Torquing Connectors

Over-torquing connectors is destructive; it may damage the connector center pin. Finger-tight is usually sufficient, especially on Type N connectors. Should it be necessary to use a wrench to tighten SMA or WSMA connectors, use a torque wrench that breaks at 8 inch-pounds. As a general rule, *never use pliers to tighten connectors.*

Table C-1. *Connector Pin-Depth Tolerance*

Port/ Conn. Type	Pin Depth (MILS)	Gauge Reading
GPC-7	+0.000 –0.003	Same As Pin Depth
N Male	20 –0.000 7 +0.004	20 +0.000 7 –0.004
N Female	20 –0.004 7 +0.000	Same As Pin Depth
3.5 mm Male, Female	–0.000 +0.002	
K Male, Female	+0.0000 –0.0035	

Teflon Tuning Washers

The center conductor on many precision connectors contains a small teflon tuning washer located near the point of mating (interface). This washer compensates for minor impedance discontinuities at the interface. The washer's location is critical to the connector's performance. *Do not disturb it.*

Avoid Mechanical Shock

Precision connectors are designed to withstand years of normal bench handling. Do not drop or otherwise treat them roughly. They are laboratory-quality devices, and like other such devices, they require careful handling.

Keep Connectors Clean

The precise geometry that makes a precision connector's high performance possible can be disturbed by dirt and other contamination adhering to connector interfaces. When not in use, keep the connectors covered.

Visual Inspection Precision connectors should be inspected periodically. Check for the following:

- Bent or broken center pin
- Damaged threads
- Other bent or damaged connector parts
- Dirt or foreign material in connector cavity.

C-3 REPAIR/ MAINTENANCE

ANRITSU recommends that no maintenance other than cleaning be attempted by the customer. Any device with a suspected defective connector should be returned to ANRITSU for repair and/or service when needed.

Appendix D
Performance Specifications

SYSTEM PERFORMANCE

Frequency Range:
37147A 22.5 MHz to 20 GHz
37169A 22.5 MHz to 40 GHz

Dynamic Range:
"Receiver Dynamic Range" is defined as the ratio of the maximum signal level for 0.1 dB compression at a sampler input a_1 , a_2 , b1, or b_2, to the noise floor. In preparing the table, 10 Hz IF bandwidth and 512 averages were used.

Model	Freq (GHz)	Max Signal Into a_x, b_x (dBm)	Noise Floor (dBm)	Receiver Dynamic Range (dB)	Source Power (dBm, Typical)
37147A	0.0225	–12	–116	104	+10
	2	–12	–106	94	+8
	20	–12	–103	91	+5
37169A	0.0225	–12	–65	104	+10
	2	–12	–93	94	+8
	20	–12	–90	91	3
	40	–15	–83	85	–3

High Level Noise (typical):
<0.03 dB and <0.4 degrees peak-to-peak variation in a 1 kHz IF bandwidth up to 20 GHz. <0.08 dB and <0.5 degrees peak-to-peak variation up to 40 GHz.

MEASUREMENT CAPABILITIES

Number of Channels: Four independent measurement channels.

Parameters: S11, S21, S22, S12, or user-defined combinations of a1, a2, b1, and b2. All measurements are made without the need to manually reverse the test device. A reflectometer setup at the front end of the receiver is required for S-parameter measurements.

Measurement Frequency Range: Frequency range of measurement can be narrowed within the calibration range without recalibration. CW mode permits single frequency measurements, also without recalibration. In addition, the system accepts N discrete frequency points where 2<N<1601.

Domains: Frequency Domain, CW Draw, and optional High Speed Time (Distance) Domain.

Formats: Log Magnitude, Phase, Log Magnitude and Phase, Smith Chart (impedance), Smith Chart (Admittance), Linear Polar, Log Polar, Group Delay, Linear Magnitude, Linear Magnitude and Phase, Real, Imaginary, Real and Imaginary, SWR, Power.

Data Points: 1601 maximum. Data points can be switched to a value of 801, 401, 201, 101, or 51 points without recalibration (if 1601 points were used in the calibration). In addition, the system accepts an arbitrary set of N discrete data points where: 2<N<1601. CW mode permits selection of a single data point without recalibration.

Reference Delay: Can be entered in time or in distance (when the dielectric constant is entered). Automatic reference delay feature adds the correct electrical length compensation at the push of a button. Software compensation for the electrical length difference between reference and test is always accurate and stable since measurement frequencies are always synthesized. In addition, the system compensates reference phase delay for dispersive transmission media, such as waveguide and microstrip.

Markers: Six independent markers can be used to read out measurement data. In delta-reference marker mode, any one marker can be selected as the reference for the other five. Markers can be directed automatically to the minimum or maximum of a data trace.

Enhanced Markers: Marker search for a level or bandwidth, displaying an active marker for each channel, and discrete or continuous (interpolated) markers.

Marker Sweep: Sweeps upward in frequency between any two markers. Recalibration is not required during the marker sweep.

Limit Lines: Either single or segmented limit lines can be displayed. Two limit lines are available for each trace.

Single Limit Readouts: Interpolation algorithm determines the exact intersection frequencies of test data and limit lines.

Segmented Limit Lines: A total of 20 segments (10 upper and 10 lower) can be generated per data trace. Complete segmented traces can be offset in both frequency and amplitude.

Test Limits: Both single and segmented limits can be used for PASS/FAIL testing. The active channel's PASS or FAIL status is indicated on CRT after each sweep. In addition, PASS/FAIL status is output through the rear panel I/O connector as selectable TTL levels (PASS=0V, FAIL=+5V, or PASS=+5V, FAIL=0V).

Tune Mode: Tune Mode optimizes sweep speed in tuning applications by updating forward S-parameters more frequently than reverse ones. This mode allows the user to select the ratio of forward sweeps to reverse sweeps after a full

12-term calibration. The ratio of forward sweeps to reverse sweeps can be set anywhere between 1:1 to 10,000:1.

DISPLAY CAPABILITIES

Display Channels: Four, each of which can display any S-parameter or user defined parameter in any format with up to two traces per channel for a maximum of eight traces simultaneously. A single channel, two channels (1 and 3, or 2 and 4), or all four channels can be displayed simultaneously. Channels 1 and 3, or channels 2 and 4 can be overlaid.
Monitor: Color, 7.5-inch diagonal, VGA display or 8.4-inch diagonal LCD. The default color configuration is as follows: graticules are displayed in green, measurement data in red, markers and limits in blue, and overlaid trace data in yellow. Trace data stored in memory are displayed in green.
Trace Color: The color of display traces, memory, text, markers and limit lines are all user definable.
Trace Overlay: Displays two data traces on the active channel's graticule simultaneously. The overlaid trace is displayed in yellow and the primary trace is displayed in red.
Trace Memory: A separate memory for each channel can be used to store measurement data for later display or subtraction, addition, multiplication or division with current measurement data.
Scale Resolution (minimum):
- **Log Magnitude:** 0.001 dB/div
- **Linear Magnitude:** 1 pU
- **Phase:** 0.01^{o}
- **Group Delay:** 0.001 ps
- **Time:** 0.001 ms
- **Distance:** 0.1 µm
- **SWR:** 1 pU
- **Power:** 0.05 dB
- **Autoscale:** Automatically sets Resolution and Offset to fully display measurement data.

Reference Position: Can be set at any graticule line.
Annotation: Type of measurement, vertical and horizontal scale resolution, start/stop or center/span frequencies, and reference position.
Blank Frequency Information: Blanking function removes all references to displayed frequencies on the CRT. Frequency blanking can only be restored through a system reset or GPIB command.

MEASUREMENT ENHANCEMENT

Data Averaging: Averaging of 1 to 4096 averages can be selected. Averaging can be toggled on/off with front panel button. A front panel button turns data averaging on/off, and a front panel LED indicates when averaging is active.
Video IF Bandwidth: Front panel button selects four levels of video IF bandwidth. MAXIMUM (10 kHz), NORMAL (1 kHz), REDUCED (100 Hz) and MINIMUM (10 Hz).
Trace Smoothing: Functions similarly to Data Averaging but computes an average over a percentage range of the data trace. The percentage of trace to be smoothed can be selected from 0 to 20% of trace. Front panel button turns smoothing on/off, and front panel LED indicates when smoothing is active.

SOURCE CONTROL

Frequency Resolution: 1 kHz (1 Hz standard on RF units and optional on Microwave units - Option 3)
Source Power Level: The source power (dBm) may be set from the 371XXA front panel menu or via GPIB. Port 1 power level is settable from +10 dB above to –20 dB below rated power (+20 dB above rated power for the 37169A) with 0.05 dB resolution. Source power ABOVE 0 dB control is allowed but not guaranteed.
Power Accuracy: ⌠0.5 dB at 2 GHz at default power.
Level Test Port Power: The power, at all sweep frequencies, is leveled to within
- ⌠1.5dB (0.0225–13.5 GHz)
- ⌠2.0dB (13.5–20 GHz)
- ⌠3.0 dB (20–40 GHz)

Power Meter Correction: The 371XXA offers a user-selectable feature that corrects for test port power variations and slope (on Port 1) using an external Hewlett-Packard 437B or Anritsu ML8403 power meter. Power meter correction is available at a user-selectable power level, if it is within the power adjustment range of the internal source. Once the test port power has been flattened, its level may be changed within the remaining power adjustment range of the signal source.
Set-On Receiver Mode: The 371XXA can be configured to measure the relative harmonic level of test devices with Set-On Receiver Mode capability. The 371XXA's unique phase locking scheme allows it to operate as a tuned receiver by locking all of its local oscillators to its internal crystal reference oscillator. Set-On Receiver Mode capability significantly increases the versatility of the 371XXA VNA in applications that check for harmonics, intermodulation products, and signals of known frequency.
Multiple Source Control Capability: Multiple Source Control capability allows a user to independently control the frequencies of two sources and the receiver without the need for an external controller. The frequency ranges and output powers of the two sources may be specified. A frequency sweep may be comprised of up to five separate bands, each with independent source and receiver settings, for convenient testing of frequency translation devices such as mixers. Up to five sub-bands may be tested in one sweep. This feature enables users to easily test mixers, up/down converters, multipliers, and other frequency conversion devices.
- **Source 1:** The 371XXA internal source or any of ANRITSU's family of 68XXXB, 69XXXA, or 6700B synthesizers.
- **Source #2:** Any of ANRITSU's family of 68XXXB, 69XXXA, or 6700B synthesizers.
- **Sweep Type:** Linear, CW, Marker, or N-Discrete point sweep.

POWER RANGE

Model	Rated Power (dbm)	Minimum Power (dBm)	Resolution (dB)
37147A	+5	–15	0.05
37169A	–3	–23	0.05

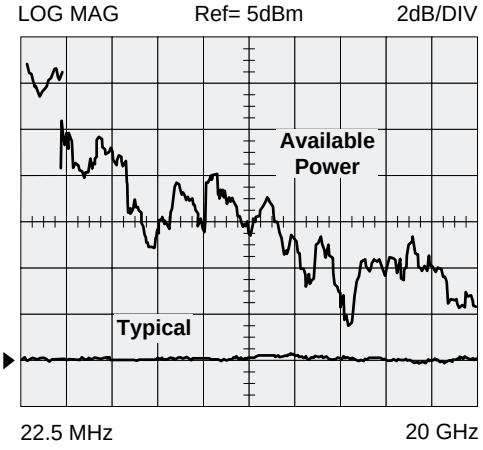
SOURCE PURITY

(Specifications apply for all models at maximum rated power.)

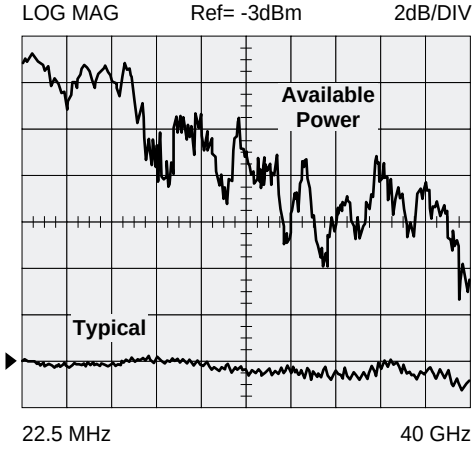
Harmonics & Harmonic Related: 35 dBc (standard)

Nonharmonics: 35 dBc

Phase Noise: >60 dBc/Hz at 10 kHz offset and 20 GHz center frequency



Model 37147A Source Power



Model 37169A Source Power

SOURCE FREQUENCY ACCURACY

Standard Time Base:

Aging: <1 x 10^{-6}/year

Stability: <1 x 10^{-6} over +15°C to +50°C range

High Stability Time Base (Option 10):

Aging: <1 x 10^{-9}/day

Stability: <5 x 10^{-9} over 0°C to +55°C range

GROUP DELAY CHARACTERISTICS

Group Delay is measured by computing the phase change in degrees across a frequency step by applying the formula:

$$\tau_g = -\frac{1}{360}\frac{d\Phi}{df}$$

Aperture: Defined as the frequency span over which the phase change is computed at a given frequency point. The aperture can be changed without recalibration. The minimum aperture is the frequency range divided by the number of points in calibration and can be increased to 20% of the frequency range without recalibration. The frequency width of the aperture and the percent of the frequency range are displayed automatically.

Range: The maximum delay range is limited to measuring no more than (180° of phase change within the aperture set by the number of frequency points. A frequency step size of 100 kHz corresponds to 10 ms.

Measurement Repeatability (sweep to sweep): For continuous measurement of a through connection, RSS fluctuations due to phase and FM noise are:

$$\frac{141\,[\,(\,\textit{Phase Noise in deg}\,)^2 + (\,\tau_g \times \textit{Residual FM Noise in Hz}\,)^2\,]^{0.5}}{360\,(\,\textit{Aperture in Hz}\,)}$$

Accuracy:

$$\textit{Error in } \tau_g = \frac{\textit{Error in Phase (deg)}}{360} + [\,\tau_g \times \textit{Aperture Freq. Error (Hz)}\,]$$
$$\textit{Aperture (Hz)}$$

VECTOR ERROR CORRECTION

Calibration can only be performed after setting a reflectometer setup at the front end of the receiver.

There are three methods of calibration:

1) Open-Short-Load (OSL). This calibration method uses short circuits, open circuits, and terminations (fixed or sliding)

2) Offset-Short (waveguide): This calibration method uses short circuits and terminations.

3) LRL/LRM: The Line-Reflect-Line (LRL) or Line-Reflect-Match (LRM) calibration uses transmission lines and a reflective device or termination (LRM).

There are four vector error correction models available:

1) Full 12-Term
2) One Path/Two Port
3) Frequency Response (Transmission/Reflection)
4) Reflection Only

Full 12-term can always be used, if desired, since all 371XXA-series models automatically reverse the test signal. Front-panel display indicates the type of calibration stored in memory. Front-panel button selects whether calibration is to be applied, and an LED lights when error correction is being applied.

Calibration Sequence: Prompts the user to connect the appropriate calibration standard to Port 1 and/or Port 2. Calibration standards may be measured simultaneously or one at a time.

Calibration Standards: For coaxial calibrations the user selects SMA, GPC-3.5, GPC-7, Type N, 2.4 mm, TNC, or K Connector from a calibration menu. Use of fixed or sliding loads can be selected for each connector type. User defined calibration standards allow for entry of open capacitance, load and short inductances, load impedance, and reflection standard offset lengths.

Reference Impedance: Modify the reference impedance of the measurement to other than 50 ohms (but not 0).

LRL/LRM Calibration Capability: The LRL calibration technique uses the charactersitic impedance of a length of transmission line as the calibration standard. A full LRL calibration consists merely of two transmission line measurements, a high reflection measurement, and an isolation measurement. The LRM calibration technique is a variation of the LRL technique that utilizes a precision termination rather that a second length of transmission line. A third optional standard, either Line or Match, may be measured in order to extend the frequency range of the calibration. This extended calibration is achieved by mathematically concatenating either two LRL, two LRM, or one LRL and one LRM calibration(s). Using these techniques, full 12-term error correction can be performed on the 371XXA VNA.

Adapter Removal Calibration: Built-in Adapter Removal application software accurately characterizes and "removes" any adapter used during calibration what will not be used for subsequent device measurements. This technique allows for accurate measurement of non-insertable devices.

Dispersion Compensation: Selectable as Coaxial (non-dispersive), Waveguide, or Microstrip (dispersive).

Reference Plane: Selectable as Middle of line 1 or Ends of line 1.

Corrected Impedance: Determined by Calibration Standards.

HARD COPY

Printer: Menu selects full screen, graphical, tabular data, S2P or Text output, and printer type. The number of data points of tabular data can be selected as well as data at markers only. Compatible with the 2225C InkJet, HP QuietJet, HP 310/320/340 DeskJet, HP 500 Deskjet, HP 560C DeskJet (b/w only), HP LaserJet II, III, & IV Series, and some Epson compatible printers with Parallel (Centronics) interfaces.

GPIB Plotters: The 371XXA VNA is compatible with HP Models 7440A, 7470A, 7475A, and 7550A (in standard mode) and Tektronix Model HC100 plotters. Menu selects plotting of full or user-selected portions of graphical data. Plotter is connected to the dedicated GPIB bus.

Performance: After selecting the Start Print button, front panel operation and measurement capability is restored to the user within 2 seconds.

STORAGE

Internal Memory: Ten front panel states (setup/calibration) can be stored and recalled from non-volatile memory locations. The current front panel setup is automatically stored in non-volatile memory at instrument power-down. When power is applied, the instrument returns to its last front panel setup.

Internal Hard Disk Drive: Used to store and recall measurement and calibration data and front-panel setups. All files are MS-DOS compatable. File names can be 1 to 8 characters long, and must begin with a character, not a number. Extensions are automatically assigned.

External SCSI Interface: Option 4 deletes the internal hard disk drive, and adds a SCSI Interface connector to the rear panel for connecting a SCSI-2 formatted hard disk drive.

Internal Floppy Disk Drive: A 3.5-inch diskette drive with 1.44 Mbytes formatted capacity is used to load measurement programs and to store and recall measurement and calibration data and front panel setups. All files are MS-DOS compatable. File names can be 1 to 8 characters long, and must begin with a character, not a number. Extensions are automatically assigned.

Measurement Data: 102.8 kbytes per 1601 point S-parameter data file.

Calibration Data: 187.3 kbytes per 1601 point S-parameter data file (12-term cal plus setup).

Trace Memory File: 12.8 kbytes per 1601 point channel.

GPIB

GPIB INTERFACES - 2 PORTS

System GPIB (IEEE-488.2): Connects to an external controller for use in remote programming of the network analyzer. Address can be set from the front panel and can range from 1 to 30.

Interface Function Codes: SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP1, DT1, DC0, C0.

Dedicated GPIB: Connects to external peripherals for network analyzer controlled operations (e.g. GPIB plotters, frequency counters, frequency synthesizers, and power meters).

GPIB Data Transfer Formats: ASCII, 32-bit floating point, or 64-bit floating point. 32-bit and 64-bit floating point data can be transferred with LSB or MSB first.

GPIB DATA COLLECTION SUMMARY

Fast CW Operation:
Fast CW is an ideal mode of operation for rapid data taking over GPIB. To achieve a fast measurement rate the display is not updated and only the raw S-parameter or user-defined parameter of the active channel is measured.

Fast CW Typical Performance

Trigger Mode	Measurement Speed (ms/point)
GPIB	1.6
External TTL	1.3
Internal	1.0

Internal Buffer Data Collection:
Internal Buffer Data Collection is provided to allow saving active channel measurement data from multiple sweeps without having to synchronize and collect data at the end of each sweep. The 37100A can store up to 20,000 data point measurements, each consisting of two (real and imaginary) IEEE 754 4-byte floating point numbers.
Throughput measurements were made as follows: start the timer, trigger a sweep, wait for a full sweep, transfer data across the GPIB and stop the timer.

Data Transfer Speed (with or without cal):
100 kbyte/sec

Measurement conditions:
22.5 MHz to 20 GHz sweep, single channel, log magnitude display, 10 kHz IF bandwidth, and output final data.

Throughput Times (ms) without Correction (typical)

Data Format	3 Points*	101 Points	401 Points	1601 Points
32 Bit	270	600	1250	3600
64 Bit	300	600	1350	4000
ASCII	300	700	1700	5000

*3 data point sweeps taken at 2, 4, and 6 GHz

GENERAL

37100A Front Panel Connectors and Controls:

Keyboard Input: An IBM-AT compatible keyboard can be connected to the front panel for navigating through front panel menus and disk directories, annotation of data files and display labels, printing displays and pausing instrument sweeps.

Source Input Loop: Provides external source input capability, replacing the internal source.

RF Output: K, female, provides source RF output.

a 1 , a 2 , b 1 , b 2 Inputs: K, female, provide inputs to the samplers.

Source Lock Output: Provides a sample of the internal source at -9 dB (typ.) relative to the internal source power.

37100A Rear Panel Connectors and Controls:

CRT BRT: Continuous control of CRT intensity (not active with LCD).

CRT DEGAUSS: Pushbutton control degausses CRT (not active with LCD).

PRINTER OUT: Centronics interface for an external printer.

VGA OUT: Provides VGA output of 371XXA video display.

10 MHz REF IN: Connects to external reference frequency standard, 10 MHz, +5 to –5 dBm, 50 ohms, BNC female.

10 MHz REF OUT: Connects to internal reference frequency standard, 10 MHz, 0 dBm, 50 ohms, BNC female.

EXT ANALOG OUT: –10V to +10V with 5 mV resolution, varying in proportion to user-selected data (e.g., frequency, amplitude). BNC female.

EXT ANALOG IN: ∫ 50 volt input for displaying external signals on the CRT in Diagnostics mode. BNC female.

LINE SELECTION: Power supply automatically senses 100V, 120V, 220V or 240V lines.

EXTERNAL TRIGGER: External triggering for 371XXA measurement, ∫1V trigger. 10 kohm input impedance. BNC female.

EXTERNAL SCSI: Provides SCSI-2 connector for connection of an external SCSI hard disk drive (Opt. 4).

EXTERNAL I/O: 25-pin DSUB connector.

LIMITS PASS/FAIL: Selectable TTL levels (Pass=0V, Fail=+5V or Pass=+5V, Fail=0V. Additionally, 0 volts (all displayed channels pass) or +5V (any one of 4 displayed channels fail) output pass/fail status (1 line).

EXTERNAL TRIGGER: External triggering for 371XXA measurement, ∫1V trigger. 10 kohm input impedance. BNC female.

EXT ANALOG OUT: –10V to +10V with 5 mV resolution, varying in proportion to user-selected data (e.g., frequency, amplitude). BNC female.

Port 1 SOURCE ATTENUATOR: Drive signal for a source external programmable step attenuator.

Port 2 TEST ATTENUATOR: Drive signal for a test external programmable step attenuator.

TRANSFER SWITCH: Drive signal for an external transfer switch.

Power Requirements: 85-240V, 48-63 Hz, 540 VA maximum

Dimensions: 267H x 432W x 585D mm (10.5H x 17W x 23D in.)

Weight: 34 kg (75 lb) - Maximum amount specified for 2-man lift requirement.

ENVIRONMENTAL

Storage Temperature Range: –40⊃C to +75⊃C

Operating Temperature Range: –0⊃C to +50⊃C

Relative Humidity: 5% to 95% at +40⊃C

EMI: Meets the emissions and immunity requirements of
EN55011/1991 Class A/CISPR-11 Class A
EN 50082-1/1993
IEC 801-2/1984 (4 kV CD, 8kV AD)
IEC 1000-4-3/1995 (3 V/m, 80-1000 MHz)

IEC 801-4/1988 (500V SL, 1000V PL)
IEC 1000-4-5/1995 (2 kV L-E, 1kV L-L)

HIGH SPEED TIME (DISTANCE) DOMAIN MEASUREMENT CAPABILITY (OPTION 2A)

Option 2A, High Speed Time (Distance) Domain software allows the conversion of reflection or transmission measurements from the frequency domain to the time domain. Measured S-parameter data is converted to the time domain by application of a Fast Fourier Transform (FFT) using the Chirp Z-Transform technique. Prior to conversion any one of several selectable windowing functions may be applied. Once the data is converted to the time domain, a gating function may be applied to select the data of interest. The processed data may then be displayed in the time domain with display start and stop times selected by the user or in the distance domain with display start and stop distance selected by the user. The data may also be converted back to the frequency domain with a time gate to view the frequency response of the gated data.

Lowpass Mode: This mode displays a response equivalent to the classic TDR (Time Domain Reflectometer) response of the device under test. Lowpass response may be displayed in either the impulse or step mode. This type of processing requires a sweep over a harmonic series of frequencies and an extrapolated or user-entered DC value.

Bandpass Mode: This mode displays a response equivalent to the time response of the device under test to a band limited impulse. This type of processing may be used with any arbitrary frequency sweep range, limited only by the test set range or device under test response.

Phasor Impulse Mode: This mode displays a response similar to the Lowpass impulse response, using data taken over an arbitrary (band limited) sweep range. Detailed information, similar to that contained in the lowpass impulse response may be used to identify the nature of impedance discontinuities in the device under test. Now, with Phasor Impulse, it is possible to characterize complex impedances on band-limited devices.

Windowing: Any one of four window functions may be applied to the initial frequency data, to counteract the effects of processing data with a finite bandwidth. These windows provide a range of tradeoffs of main lobe width versus sidelobe level (ringing).

The general type of function used is the Blackman-Harris window with the number of terms being varied from one to four. Typical performance follows:

Types of Window (Number of Terms)	First Side Lobe Relative to Peak	Impulse Width[ά]
Rectangular (1)	–13 dB	1.2W
Nominal-Hamming (2)	–43 dB	1.8W
Low Side Lobe, Blackman-Harris (3)	–67 dB	2.1W
Minimum Side Lobe, Blackman-Harris (4)	–92 dB	2.7W

ά W(Bin Width) = 1/2Δf sweep width
Example: When Δf = 40 MHz to 40 GHz, W = 12.5 ps

Gating: A selective gating function may be applied to the time domain data to remove unwanted responses, either in a pass-band or reject-band (mask). This gating function may be chosen as the convolution of any of the above window types with a rectangular gate of user defined position and width. The gate may be specified by entering start and stop times or center and span. The gated data may be displayed in the time domain, or converted back to the frequency domain.

Time Domain Display: Data processed to time domain may be displayed as a function of time or as a function of distance, provided the dielectric constant of the transmission media is entered correctly. In the case of dispersive media such as waveguide or microstrip, the true distance to a discontinuity is displayed in the distance mode. The time display may be set to any arbitrary range by specifying either the start and stop times or the center time and span. The unaliased (non-repeating) time range is given by the formula:

$$UnaliasiedRange\ (ns) = \frac{Number\ of\ Frequency\ Data\ Points}{Frequency\ Sweep\ Range\ (GHz)}$$

The resolution is given by the formula:

$$Main\ Lobe\ Width\ (null - null)\ in\ ns = \frac{kW}{Freq.Sweep\ Range\ (GHz)}$$

Where kW is two times the number of window terms (for example, four for a two-term window)

For a 40 GHz sweep range with 1601 data points, the unaliased range is 40.025 nanoseconds.

Frequency with Time Gate: Data that has been converted to time domain and selected by the application of gating function may be converted back to the frequency domain. This allows the display of the frequency response of a single element contained in the device under test. Frequency response accuracy is a function of window and gate type, and gate width. For a full reflection, minimum gate and window accuracy is within 0.2 dB of the ungated response over a 40 GHz range.

SYSTEM OPTIONS

OPTION 1, Rack Mounting:
Rack mount kit containing a set of track slides (90 tilt capability), mounting ears, and front panel handles to let the instrument be mounted in a standard 19-inch equipment rack.
OPTION 1A, Rack Mounting:
Rack mounting kit containing a set of mounting ears and hardware to permanently mount instrument in a standard 19-inch equipment rack.
OPTION 2, High Speed Time (Distance) Domain Measurement Capability
OPTION 4, External SCSI-2 Hard Disk Drive Compatibility:
Provides SCSI-2 rear panel connector for connection of an external SCSI HDD. Remove internal HDD.
OPTION 10A, High Stability Time Base and 1 Hz Frequency Resolution:
Replaces the standard temperature compensated crystal oscillator (with a temperature stability of 1ppm over a 0 to 55C range)with an ovenized crystal oscillator (aging stability of 1 x 10-9/day and temperature stability 5 x 10-9 over 0 to 55C range). Also, adds 1 Hz frequency resolution.
OPTION 13, Delete Source:
Allows the removal of the internal source for applications where only external sources are required.

UPGRADE OPTIONS*

ND44587
Upgrade 37147A to 37169A

Consult with Anritsu ANRITSU for other available upgrades

ON-SITE SUPPORT

Option ES 31:
3 year on-site repair.
Option ES 37:
3 year on-site verification
Option ES 38:
3 year on-site Mil-Std verification
Extended Service Options
Additional, two year and four year return to ANRITSU service is available, as an option for 37100A systems and components. Prices and details are available from your Sales Representative or by contacting the factory.

CALIBRATION KITS

Standard
3650 SMA/3.5 mm Calibration Kit
Option 1: Male and Female Sliding Terminations
3651 GPC-7 Calibration Kit
Option 1: Sliding Terminations
3652 K Connector Calibration Kit
Option 1: Male and Female Sliding Terminations
3653 Type N Calibration Kit

Economy (8.6 GHz)
3750 SMA Calibration Kit
3751 GPC-7 Calibration Kit
3753 Type N, 50 W, Calibration Kit
3753-75 Type N, 75 Ω, Calibration Kit

T/LRM
36550 3.5 mm Calibration Kit
36552 K Connector Calibration Kit
36553 Type N Calibration Kit

GPIB CABLES

2100-1 GPIB Cable, 1 m (3.3 ft.)
2100-2 GPIB Cable, 2 m (6.6 ft.)
2100-4 GPIB Cable, 4 m (13.2 ft.)
2100-5 GPIB Cable, 0.5 m (1.65 ft.)

ACCESSORIES

2000-660 HP 340 Deskjet Printer, Printer Stand, Deskjet Printer Cartridge and Power cord.
2000-661 Extra Printer Cartridge
2000-662 Rechargeable Battery
2000-663 Power Cable, Europe
2000-664 Power Cable, Australia
2000-665 Power Cable, *U.K.*
2000-666 Power Cable, Japan
2000-667 Power Cable, South Africa
2225-1 Spare Parallel Interface Printer Cable

Appendix E
Millimeter Wave Service Instructions

Contents

Appendix E
Millimeter Wave Service Instructions

E-1 INTRODUCTION

This appendix provides service instructions for the 371XXA Millimeter Wave System. The information in this appendix is peculiar to the this system and is intended to supplement the common service instructions contained in the other parts of this manual. Also, certain information in this appendix assumes that the reader is familiar with the operation of the instrument. Operating information is contained in Chapter 11 of the 371XXA OM (Part Number: 10410-00190, Revision C).

E-2 DESCRIPTION

The 371XXA Millimeter Wave System (371XXAmm) consists of a 37147A or 37169A VNA, two 680XXC Frequency Synthesizers, and a 3735B Millimeter Test Set having two 374X Millimeter Wave Modules. There are 14 different 374X modules available (below) to accommodate different measurement types and frequency ranges.

- 3741A-Q 3 to 50 GHz Transmission Module
- 3741A-V 50 to 75 GHz Transmission Module
- 3741A-E 60 to 90 GHz Transmission Module
- 3741A-EE56 to 94 GHz Transmission Module
- 3741A-W 75 to 110 GHz Transmission Module
- 3741A-EW 65 to 110 GHz Transmission Module
- 3741A-F 90 to 140 GHz Transmission Module
- 3740A-Q 33 to 50 GHz Transmission/Reflection Module
- 3740A-V 50 to 75 GHz Transmission/Reflection Module
- 3740A-E 60 to 90 GHz Transmission/Reflection Module
- 3740A-EE 56 to 94 GHz Transmission/Reflection Module
- 3740A-W 75 to 110 GHz Transmission/Reflection Module
- 3740A-EW 65 to 110 GHz Transmission/Reflection Module
- 3740A-F 90 to 140 GHz Transmission/Reflection Module

E-3 REPLACEABLE PARTS

The tables below supplement the parts lists in Chapter 2. See Figure E-1 for parts locations.

Table E-1. *3735B Millimeter Test Set Assemblies / Parts*

Assembly / Part	Part Number
3735B Power Supply	40-130
Rear Panel Transfer Switch PCB Assembly	B45390
Transfer Switch Assmbly, harnessed	B45396
Power Distribution PCB Assembly	D45631-3
Isolator	1000-49
Power Divider	1091-87
Fan Assembly	B45397
Line Module	260-34
Panel Connectors	B15660

Table E-2. *Miscellaneous Assemblies*

Assembly / Part	Part Number
Test Set / Module Interface Cable	47958
VNA / Test Set Transfer Switch Interface Cable	B46743
VNA / Test Set RF Cable	ND46618
Test Set / Source 1 RF Cable	ND44620
Test Set / Source 2 RF Cable	ND44621
GPIB Interface Cable, 2 meter	2100-2

E-4 PERFORMANCE VERIFICATION– GENERAL

General instructions for performing performance verification procedures are provided below .

Required Equipment

The following equipment is required to perform the verification tests:

Model	Description	Quantity
Anritsu 3655 Series	Waveguide Calibration Kit, with Option 1: Sliding Termination	1

Initial System Setup

Set up the equipment as described below.

Step 1. Remove the silver straight waveguide sections from the modules.

Step 2. Install the precision-straight waveguide sections that are contained in the calibration kit on the waveguide output connector of each millimeter module.

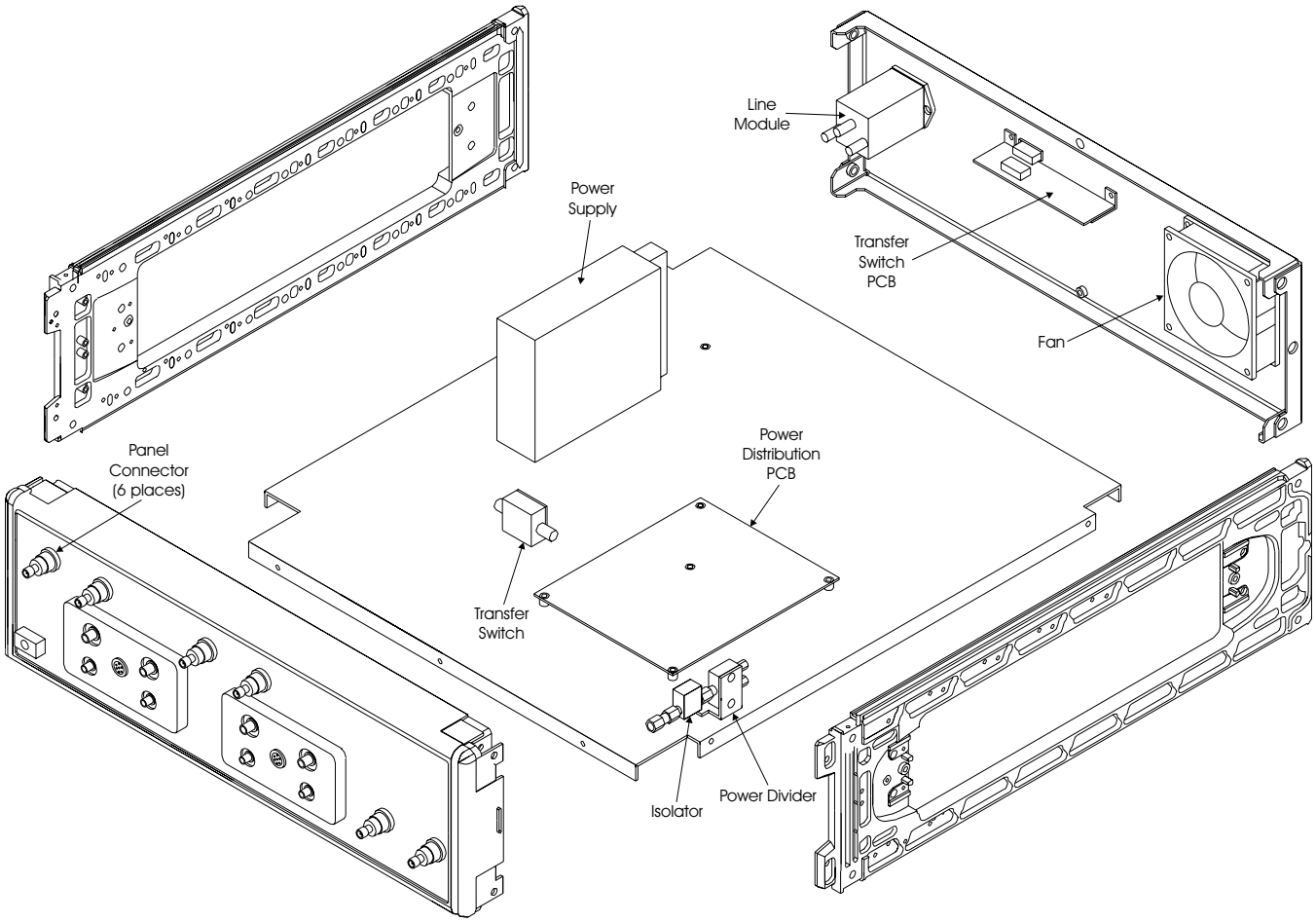


Figure E-1. *Parts Locations*

MENU OPTNS
OPTIONS
TRIGGERS
REAR PANEL OUTPUT
Millimeter Wave BAND DEFINITION
RECEIVER MODE
SOURCE CONFIG
TEST SET CONFIG
PRESS <ENTER> TO SELECT

NOTE

These waveguide sections (test port adapters) use high precision flanges to improve connection repeatability and calibration quality. They *must* be used to ensure specified system performance.

Step 3. Apply power to the synthesizers and then the network analyzer.

Step 4. Press Option Menu, select TEST SET CONFIG from the displayed men (left) to configure the system for the types of millimeter modules used.

Step 5. Allow the system to warm up for at least 60 minutes to ensure operation to performance specifications.

E-5 PERFORMANCE VERIFICATION–IF POWER LEVEL TEST

This test verifies that each individual receiver channel operates properly. Measurement calibration of the system is not required for this test.

Test Setup Set up the test equipment as described below.

Step 1. Install a flush short on the output of the 3740A-X module to PORT 1.

Step 2. Set up the network analyzer as shown below.

Key	Menu Choice
SETUP MENU	START: Low-end Frequency STOP: High-end Frequency
CHANNEL MENU	DUAL CHANNELS 1 & 3
GRAPH TYPE	LOG MAGNITUDE (both channels)
S-PARAMS	Channel 1 User Ratio: a1/1 User Phase Lock: a1 Channel 3 User Ratio: b1/1 User Phase Lock: a1
SET SCALE	RESOLUTION: 10.0 dB/DIV REF VALUE: -10.0 dB (both channels)
LIMITS	UPPER LIMIT ON See Note below LOWER LIMIT ON See note below (both channels) *Note: Refer to Table E-3 for limit line settings*

Table E-3. *Limit Line Settings*

Limit Type	Model and Frequency Range (GHz)									
	3740A-Q 33-50	3740A-V 50-75	3740A-E 60-90	3740A-EE 56-60	3740A-EE 60-85	3740A-EE 85-94	3740A-W and 3740A-EW 65-75	3740A-W and 3740A-EW 75-100	3740A-W and 3740A-EW 100-110	3740A-F 90-140
a1/1 (a2/1) UPPER LIMIT dB	–5	–5	–5	–5	–5	–5	–5	–5	–5	–5
a1/1 (a2/1) LOWER LIMIT dB	–29	–27	–29	–34	–29	–39	–39	–27	–34	–39
b1/1 (b2/1) UPPER LIMIT dB	–2	–2	–2	–2	–2	–2	–2	–2	–2	–2
b1/1 (b2/1) LOWER-LIMIT dB	–26	–24	–26	–31	–26	–36	–36	–21	–31	–36

Test Procedure The test procedure is given below.

Step 1. Observe sweep indicator and allow at least one complete sweep to occur.

Step 2. Verify that the measurement traces fall within the limit lines.

Step 3. If the second module connected to Port 2 is also a Model 3740A-X Transmission/Reflection module, change setup to that shown in below and perform step 4. Otherwise, skip to step 6.

Key	Menu Choice
CHANNEL MENU	DUAL CHANNELS 2 & 4
S-PARAMS	Channel 2 User Ratio: a2/1 User Phase Lock: a2 Channel 4 User Ratio: b2/1 User Phase Lock: a2

Step 4. Install a flush short to the output of the 3740A-X module on Port 2.

Step 5. Verify that the measurement traces fall within the limit lines.

Step 6. If the second module to be tested is a Model 3741A-X, connect the two modules together and change the setup to that shown below.

Key	Menu Choice
CH 3	ON
CHANNEL MENU	SINGLE CHANNEL
S-PARAMS	Channel 3
	User Ratio: b2/1
	User Phase Lock: a1

Step 7. Verify that the measurement trace falls within the limit lines.

E-6 PERFORMANCE VERIFICATION–HIGH LEVEL NOISE TEST, TRANSMISSION

The following test verifies that the high-level noise in the 371XXA Millimeter VNA System will not significantly affect the accuracy of subsequent measurements. High-level noise is the random noise that exists in the 371XXA Millimeter VNA System. Because it is non-systematic, it cannot be accurately predicted or measured. Thus, it cannot be removed using conventional error-correction techniques. Measurement calibration is not required for this test.

NOTE

This test is not applicable if you are only using a single 3740A-X module on Port 1.

Test Setup Set up the 371XXA Millimeter VNA System as shown on the following page.

Key	Menu Choice
SETUP MENU	START: Low-end Frequency STOP: High-end Frequency
CHANNEL MENU	DUAL CHANNELS 1 & 3 (two 3740A-X's) SINGLE CHANNEL 3 (one 3740A-X and one 3741A-X)
GRAPH TYPE	LOG MAGNITUDE (Both channels)
SET SCALE	RESOLUTION: 0.050 dB/DIV REF VALUE: 0.0 dB (Both channels)
S-PARAMS	Channel 1 - S12 Channel 3 - S21
DATA POINTS	401
VIDEO IF BW	1 KHz
LIMITS	UPPER LIMIT ON 0.010 dB (Q Band) 0.025 dB (V Band) 0.030 dB (E Band) 0.040 dB (Extended E Band) 0.030 dB (W Band) 0.040 dB (Extended W Band) 0.040 dB (F Band) LOWER LIMIT ON -0.010 dB (Q Band) -0.025 dB (V Band) -0.030 dB (E Band) -0.040 dB (Extended E Band) -0.030 dB (W Band) -0.040 dB (Extended W Band) -0.040 dB (F Band)

Test Procedure The test procedure is given below.

MENU NO1
TRACE MEMORY FUNCTIONS
VIEW DATA
VIEW MEMORY
VIEW DATA AND MEMORY
VIEW DATA (/) MEMORY
SELECT TRACE MATH
STORE DATA TO MEMORY
DISK OPERATIONS
PRESS <ENTER> TO SELECT

Step 1. Connect the two modules together.

Step 2. If using two 3740A-X's, press Ch 1 key and perform step 3 through 9. Otherwise, go to step 10.

Step 3. Press Trace Memory.

Step 4. Choose VIEW DATA from menu (left) and press Enter.

Step 5. While observing sweep indicator, allow at least two complete sweeps to occur. (One complete sweep if using single channel display.)

Step 6. Choose STORE DATA TO MEMORY from menu and press Enter.

Step 7. Choose VIEW DATA (/) MEMORY from menu and press Enter.

Step 8. While observing sweep indicator, allow at least two complete sweeps to occur. (One complete sweep if using single channel display.)

Step 9. Verify that the peak-to-peak High Level Noise falls within the area between the two limit lines.

Step 10. Press Ch 3.

Step 11. Repeat step 4 through 9 for channel 3.

E-7 PERFORMANCE VERIFICATION–HIGH LEVEL NOISE TEST, REFLECTION

The following test verifies that the high-level noise in the 371XXA Millimeter VNA System will not significantly affect the accuracy of subsequent measurements. High-level noise is the random noise that exists in the 371XXA Millimeter VNA System. Because it is non-systematic, it cannot be accurately predicted or measured. Thus, it cannot be removed using conventional error-correction techniques. Measurement calibration is not required for this test.

Test Setup Setup as shown below.

Key	Menu Choice
SETUP MENU	START: Low-end Frequency STOP: High-end Frequency
CHANNEL MENU	DUAL CHANNELS 1 & 3 (two 3740A-X's) SINGLE CHANNEL 1 (one 3740A-X and one 3741A-X)
GRAPH TYPE	LOG MAGNITUDE (Both channels)
SET SCALE	RESOLUTION: 0.050 dB/DIV REF VALUE: 0.0 dB (Both channels)
S-PARAMS	Channel 1: S11 Channel 3: S22
DATA POINTS	401
VIDEO IF BW	1 KHz
LIMITS	UPPER LIMIT ON 0.010 dB (Q Band) 0.025 dB (V Band) 0.030 dB (E Band) 0.040 dB (Extended E Band) 0.030 dB (W Band) 0.040 dB (Extended W Band) 0.040 dB (F Band) LOWER LIMIT ON -0.010 dB (Q Band) -0.025 dB (V Band) -0.030 dB (E Band) -0.040 dB (Extended E Band) -0.030 dB (W Band) -0.040 dB (Extended W Band) -0.040 dB (F Band)

Test Procedure The test procedure is given below.

MENU NO1
TRACE MEMORY FUNCTIONS
VIEW DATA
VIEW MEMORY
VIEW DATA AND MEMORY
VIEW DATA (/) MEMORY
SELECT TRACE MATH
STORE DATA TO MEMORY
DISK OPERATIONS
PRESS <ENTER> TO SELECT

Step 1. Attach flush short to waveguide port on 3740A-X on Port 1 (and Port 2, if two are used); leave waveguide port on 3741A-X unterminated.

Step 2. Press Ch 1.

Step 3. Press Trace Memory.

Step 4. Choose VIEW DATA from menu and press Enter.

Step 5. While observing sweep indicator, allow at least two complete sweeps to occur. (One complete sweep if using single channel display.)

Step 6. Choose STORE DATA TO MEMORY from menu and press Enter.

Step 7. Choose VIEW DATA (/) MEMORY from menu and press Enter.

Step 8. While observing sweep indicator, allow at least two complete sweeps to occur. (One complete sweep if using single channel display.)

Step 9. Verify that the peak-to-peak High Level Noise falls within the area between the two limit lines.

Step 10. If two 3740A-X's are used, press Ch 3 and repeat step 4 through 9 for channel 3.

E-8 PERFORMANCE VERIFICATION–SYSTEM DYNAMIC RANGE TEST

This test verifies that the system meets its dynamic range specifications. Dynamic range is defined as the ratio of the power incident on Port 2 in a through line connection to the noise floor at Port 2. This definition differs slightly from the classical definition of available receiver dynamic range, which takes into account the maximum signal level at Port 2 for 0.1 dB compression.

For this test, the system *must* be calibrated and the error correction *must be applied* for this test to be valid.

NOTE

System dynamic range is not applicable if you are using a single 3740A-X module on Port 1.

Calibration Calibrate the system as described below.

Step 1. Load the Waveguide Cal Kit Component Coefficients to the 371XXA, using the Utility Menu key.

Step 2. Press Begin Cal.

Step 3. Select 12-TERM calibration if two 3740A-X's are installed; otherwise, use 1 PATH 2 PORT (8-term) calibration.

Step 4. Select the following:

INCLUDE ISOLATION
NORMAL DATA POINTS
Desired frequencies
CHANGE LOAD TYPE
SLIDING
BEGIN CAL

Step 5. Prior to measuring Isolation Devices, press Avg/Smooth Menu key, and change averaging to 512. Also, press Video IF BW key, and change to 100 Hz.

Step 6. Press Enter key to resume calibration; finish as prompted.

Step 7. Ensure that the Apply Cal key indicator is on after the calibration is complete.

Test Procedure The test procedure is given below.

Step 1. Set up the system as shown below.

Key	Menu Choice
SETUP MENU	START: Low-end Frequency STOP: High-end Frequency
CHANNEL MENU	DUAL CHANNELS 1 & 3 (two 3740A-X's) SINGLE CHANNEL 3 (one 3740A-X and one 3741A-X)
GRAPH TYPE	LOG MAGNITUDE (Both channels)
SET SCALE	RESOLUTION: 20 dB/DIV REF VALUE: 0.0 dB REFERENCE LINE: TOP (both channels)
S-PARAMS	Channel 1 - S12 Channel 3 - S21
AVG/SMOOTH MENU	AVERAGING 512 MEAS. PER POINT
AVERAGE	ON
DATA POINTS	401
VIDEO IF BW	100 Hz
LIMITS	UPPER LIMIT ON (Refer to Table E-4 for setting value)

Step 2. Attach a Termination or a sliding load to the Port 1 module waveguide output.

Step 3. Connect a precision termination to the Port 2 module waveguide output.

Step 4. While observing sweep indicator, allow at least one complete sweep to occur.

Step 5. Verify that the trace falls below the limit line at all frequencies.

Table E-4. *System Dynamic Range*

Model	Q Band	V Band	E Band	Extended E Band			W Band	Extended W Band			F Band	
Frequency Range (GHz)	33–50	50–75	60–90	56–60	60–85	85–94	75–100	65–70	75–100	100–110	90–115	115–140
System Dynamic Range (dB)	100	97	96	90	96	80	95	85	94	89	85	80

E-9 PERFORMANCE VERIFICATION–SOURCE MATCH/DIRECTIVITY TEST

This test verifies that the source match and directivity of the system meet specifications. The system *must* be calibrated and the error correction *must be applied* for these tests.

NOTE

This test is not applicable to 3741A-X module.

Test Setup

Set up test equipment as described below.

NOTE

If measurement calibration is valid, skip this section.

Step 1. Load the Waveguide Cal Kit Component Coefficients ini the 371XXA.

Step 2. Press Begin Cal.

NOTE

In next step, use 12-TERM calibration if two 3740A-X's are installed; otherwise, use 1PATH 2 PORT (8-term) calibration.

Step 3. Using the menu prompts, perform a 12 or 8 term sliding load calibration over the full system operating range.

Step 4. At the ISOLATION DEVICE menu prompt, press Avg/Smooth Menu and change averaging to 512 MEAS. PER POINT. Also, press Video IF BW and change to 100 Hz. Then press Enter to continue.

Step 5. At the SLIDING LOAD menu prompt, press Avg/Smooth Menu and change averaging to 512 MEAS. PER POINT. Also press Video IF BW and change to 100 Hz. Then press Enter to continue.

Step 6. At the BROADBAND LOAD menu prompt, press Avg/Smooth Menu and change averaging to 512 MEAS. PER POINT. Also press Video IF BW and change to 100 Hz. Then press Enter to continue.

Step 7. Ensure that the Apply Cal key indicator is on after the calibration is complete.

Test Procedure The test procedure is given below.

Step 1. Set up system as shown below.

Key	Menu Choice
SETUP MENU	START: Low-end Frequency STOP: High-end Frequency
CHANNEL MENU	SINGLE CHANNEL Channel 1
GRAPH TYPE	LOG MAGNITUDE
SET SCALE	RESOLUTION: 0.1 dB/DIV REF VALUE: 0.0 dB REFERENCE LINE: TOP
S-PARAMS	S11

Step 2. Attach a second high-precision waveguide section to the module on Port 1.

Step 3. Attach a flush short to the end of the high-precision waveguide section.

Step 4. While observing the sweep indicator, allow at least one complete sweep to occur. Press Autoscale to center the trace.

Step 5. Press Marker Menu, and select MARKER 1, MARKER 2, and MARKER 3, to be ON.

Step 6. Using the rotary knob, position marker 1 and marker 2 to adjacent peaks of the ripple with the greatest negative trough (or adjacent troughs if the ripple has the greatest positive peak); position marker 3 to the bottom of the trough (or the top of the peak if the ripple has the greatest positive peak). Refer to Figure 2 (next page).

Step 7. Using the Marker Menu and Readout Marker key menus, record the absolute value of markers 1 and 2 as follows:

- Subtract one from the other.
- Halve the difference
- Add the resultant to the value of the marker at the lowest peak (or the deepest trough).

  This is the average value of the two peaks (or troughs).

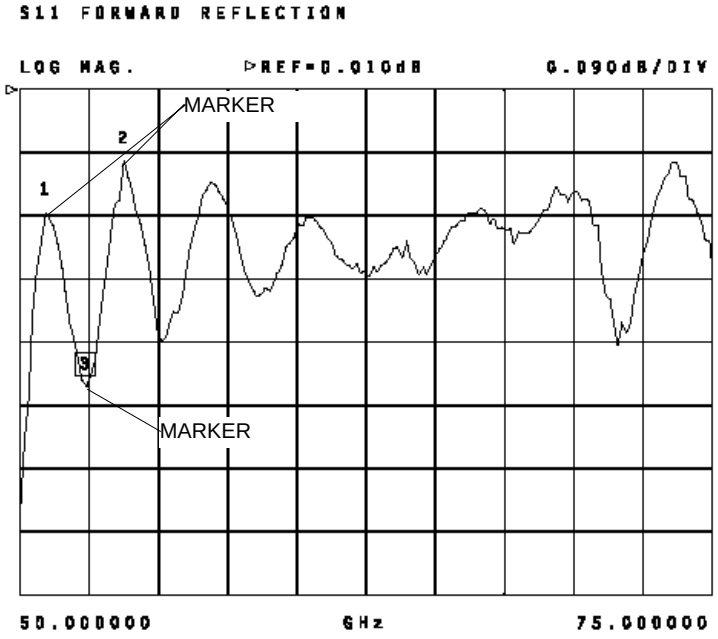


Figure E-2. *Markers*

Step 8. Record the marker 3 value.

Step 9. Find the absolute difference of the values recorded in step 7 and step 8. This is the Peak-to-Peak Ripple value. Use the RF Measurement Chart (Table E-5) to find the corresponding Return Loss value. This value is the measured effective test port match. Verify if it meets the specifications listed in Table 10.

Step 10. Remove the flush short from the end of the high-precision waveguide section. Point the test ports away from all reflective objects.

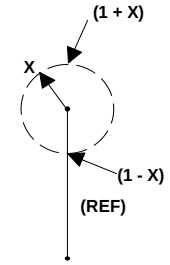
Step 11. Press Autoscale key to center the trace.

Step 12. Repeat step 6 through 8.

Step 13. Find the absolute difference of the values recorded in step 7 and step 8. This is the Peak-to-Peak Ripple value. Use the RF Measurement Chart to find the corresponding Return Loss value.

Table E-5. *RF and Microwave Measurement Chart*

Conversion tables for Return Loss, Reflection Coefficient, and SWR with tabular values for interaction of a small phasor x with a large phasor (unity reference) expressed in dB related to reference.



PHASOR INTERACTION

TERM002.DRW

SWR	Reflection Coefficient	Return Loss (dB)	Relative to Unity Reference: X dB Below Reference	Relative to Unity Reference: REF + X dB	Relative to Unity Reference: REF – X dB	Relative to Unity Reference: REF ⎛ X Peak to Peak Ripple dB
17.3910	0.8913	1	1	5.5350	–19.2715	24.8065
8.7242	0.7943	2	2	5.0780	–13.7365	18.8145
5.8480	0.7079	3	3	4.6495	–10.6907	15.3402
4.4194	0.6310	4	4	4.2489	–8.6585	12.9073
3.5698	0.5623	5	5	3.8755	–7.1773	11.0528
3.0095	0.5012	6	6	3.5287	–6.0412	9.5699
2.6146	0.4467	7	7	3.2075	–5.1405	8.3480
2.3229	0.3981	8	8	2.9108	–4.4096	7.3204
2.0999	0.3548	9	9	2.6376	–3.8063	6.4439
1.9250	0.3162	10	10	2.3866	–3.3018	5.6884
1.7849	0.2818	11	11	2.1567	–2.8756	5.0322
1.6709	0.2512	12	12	1.9465	–2.5126	4.4590
1.5769	0.2239	13	13	1.7547	–2.2013	3.9561
1.4985	0.1995	14	14	1.5802	–1.9331	3.5133
1.4326	0.1778	15	15	1.4216	–1.7007	3.1224
1.3767	0.1585	16	16	1.2778	–1.4988	2.7766
1.3290	0.1413	17	17	1.1476	–1.3227	2.4703
1.2880	0.1259	18	18	1.0299	–1.1687	2.1986
1.2528	0.1122	19	19	0.9237	–1.0337	1.9574
1.2222	0.1000	20	20	0.8279	–0.9151	1.7430
1.1957	0.0891	21	21	0.7416	–0.8108	1.5524
1.1726	0.0794	22	22	0.6639	–0.7189	1.3828
1.1524	0.0708	23	23	0.5941	–0.6378	1.2319
1.1347	0.0631	24	24	0.5314	–0.5661	1.0975
1.1192	0.0562	25	25	0.4752	–0.5027	0.9779
1.1055	0.0501	26	26	0.4248	–0.4466	0.8714
1.0935	0.0447	27	27	0.3796	–0.3969	0.7765
1.0829	0.0398	28	28	0.3391	–0.3529	0.6919
1.0736	0.0355	29	29	0.3028	–0.3138	0.6166
1.0653	0.0316	30	30	0.2704	–0.2791	0.5495
1.0580	0.0282	31	31	0.2414	–0.2483	0.4897
1.0515	0.0251	32	32	0.2155	–0.2210	0.4365
1.0458	0.0224	33	33	0.1923	–0.1967	0.3890
1.0407	0.0200	34	34	0.1716	–0.1751	0.3467
1.0362	0.0178	35	35	0.1531	–0.1558	0.3090
1.0322	0.0158	36	36	0.1366	–0.1388	0.2753
1.0287	0.0141	37	37	0.1218	–0.1236	0.2454
1.0255	0.0126	38	38	0.1087	–0.1100	0.2187
1.0227	0.0112	39	39	0.0969	–0.0980	0.1949
1.0202	0.0100	40	40	0.0864	–0.0873	0.1737
1.0180	0.0089	41	41	0.0771	–0.0778	0.1548
1.0160	0.0079	42	42	0.0687	–0.0693	0.1380
1.0143	0.0071	43	43	0.0613	–0.0617	0.1230
1.0127	0.0063	44	44	0.0546	–0.0550	0.1096
1.0113	0.0056	45	45	0.0487	–0.0490	0.0977
1.0101	0.0050	46	46	0.0434	–0.0436	0.0871
1.0090	0.0045	47	47	0.0387	–0.0389	0.0776
1.0080	0.0040	48	48	0.0345	–0.0346	0.0692
1.0071	0.0035	49	49	0.0308	–0.0309	0.0616
1.0063	0.0032	50	50	0.0274	–0.0275	0.0549
1.0057	0.0028	51	51	0.0244	–0.0245	0.0490
1.0050	0.0025	52	52	0.0218	–0.0218	0.0436
1.0045	0.0022	53	53	0.0194	–0.0195	0.0389
1.0040	0.0020	54	54	0.0173	–0.0173	0.0347
1.0036	0.0018	55	55	0.0154	–0.0155	0.0309
1.0032	0.0016	56	56	0.0138	–0.0138	0.0275
1.0028	0.0014	57	57	0.0123	–0.0123	0.0245
1.0025	0.0013	58	58	0.0109	–0.0109	0.0219
1.0022	0.0011	59	59	0.0097	–0.0098	0.0195
1.0020	0.0010	60	60	0.0087	–0.0087	0.0174

Step 14. Find the corresponding 1 + X or 1 - X value from the RF Measurement Chart. Use the following formula to calculate the effective directivity value.

For ripple with negative trough,

Step 15. *Effective Directivity =*
Return Loss value + (Absolute Value of Marker 3) - (1 - X)

For ripple with positive peak,

Effective Directivity =
Return Loss value + (Absolute Value of Marker 3) + (1 + X)

Verify if the calculated value meets the directivity specifications listed in Table E-6.

Table E-6. *Directivity and Source Match Specifications*

Model	Q Band	V Band	E Band	Extended E Band	W Band	Extended W Band	F Band
Frequency (GHz)	33 to 50	50 to 75	60 to 90	56 to 94	75 to 110	65 to 110	90 to 140
Directivity (dB)	46	46	46	44	46	40	43
Source Match (dB)	45	37	36	33	36	30	32

E-10 TROUBLESHOOTING

The 371XXA Millimeter Wave VNA System is a complex system consisting of four main component groups:

- Signal Sources
- Test Set
- Millimeter Wave Modules
- Vector Network Analyzer

A failure occurring in any of the main components will affect the operation of the entire system. Thus, it is essential to be familiar with how each component functions and how it interacts with the other components. Refer to System Description (page E-22) for a functional description of each module.

The procedures describe in this section provide a general approach to troubleshooting the 371XXA Millimeter Wave VNA System problems.

There are two basic steps for troubleshooting the 371XXA Millimeter Wave VNA System:

Define The Fault Accurately

It is no good trying to locate a fault (problem) that is vaguely defined. The symptoms must be accurately noted and this means that a functional test must be made on the system.

- What are system level symptoms?
- Which units function OK?

Isolate The Fault

Find out:

- At which sweep direction the fault occurs?
- At what frequency does the fault occur?

Determine The Fault Location

Use the following to determine the fault location.

- If the problem occurs in both sweep directions at all frequencies, the fault could be in the Signal Sources, test set or the VNA.
- If the problem occurs in both sweep directions at only certain frequencies, the fault could be in the Signal Sources.
- If the problem occurs in only one sweep direction, the fault could be in the Test Set or the Millimeter Wave Module.
- The defective component can also be isolated by substituting a known good component, swapping components, and performing the necessary tests.

If The Fault Is In The Signal Sources

Generally, a problem occurring in the Signal Source (Synthesizer) will cause the instrument to display error codes on the front panel display during the self-test routine. Refer to 680XXC/681XXC Maintenance Manual for Synthesizer problems.

If The Fault Is In The Test Set

Faults occurring in the Millimeter Wave Test Set can be divided into two types of problems:

- RF Components Problems
- PCB Assembly Problems

RF Components Check

Use the following procedure to check the RF signal paths.

Step 1. Setup equipment as shown below.

Key	Menu Choice
SETUP MENU	START: 8 GHz STOP: 20 GHz
CHANNEL MENU	DUAL CHANNELS 1 & 3
GRAPH TYPE	LOG MAGNITUDE
SET SCALE	RESOLUTION: 3.5 dB/DIV REF VALUE: 0.0 dB REFERENCE LINE: 0.0 dB (both channels)
S-PARAMS	Channel 1 - S12 Channel 3 - S21
DATA POINT	401
VIDEO IF BW	100 Hz

Step 2. Perform a Both Path Transmission Response Calibration. Refer to Chapter 7, paragraph 7-4, of the 371XXA Operation Manual.

Use a through cable to connect b1 and RF Output for forward throughline calibration and connect b2 and RF Output for reverse throughline calibration. If 371XXA includes option 13 (Deleted Source), connect to RF Output of Source 1 instead.

Step 3. Select SINGLE CHANNEL and CHANNEL 3. Measure the transmission loss for the signal paths shown below:

NOTE

When measuring RF Input to Port 2 RF Output signal path, select channel 1 and toggle the transfer switch for Port 2 signal path.

Measure Isolation between Port 1 RF Output and Port 2 RF Output. Verify if isolation is 50 dB minimum.

This can be done after RF Input to Port 1 RF Output transmission loss has been measured. Remove the cable connecting to Port 1 RF Output and then connect it to Port 2 RF Output. Leave the other connections in their original places.

Signal Paths	Transmission Loss Specifications	371XXA Channel Selection
LO Input to Port 1 LO Output	-7 dB maximum	S21
LO Input to Port 2 LO Output	-7 dB maximum	S21
RF Input to Port 1 RF Output	-4.5 dB maximum	S21
RF Input to Port 2 RF Output	-4.5 dB maximum	S12

Step 4. Replace components as follows:

- If LO Input to Port X LO Output test fails, replace the power spliter.
- If RF Input to Port X RF Output test fails, replace the transfer switch.

PCB Assembly Voltage Check

Use the following procedure to check the PCB Assembly.

Step 1. Apply Line voltage to the test set.

Step 2. Use a DMM to measure the DC voltage at each of the five test points shown below.

Measured Test Point	Reference Test Point	DC Voltage
TP2	TP1	+15.000V ±50mV
TP3	TP1	+5.00V ±0.2V
TP4	TP1	<0.3V
TP5	TP1	<0.3V

Step 3. Replace components as follows:

- If fails, replace the Power Distribution PCB Assembly.
- If the step 3 does not correct the problem, replace 40-127 Power Supply.

If The Fault Is In The Millimeter Wave Module:

A problem occurring in the millimeter wave module will usually show up in the IF Power Level Test (page E-4).

- One of the troubleshooting tools is to switch the suspect module and its associated interface cable from Port 1 to Port 2 or vice versa and check if the problem migrates to the other Port.
  - If yes, then switch the associated interface cables.
- Check again if the problem migrates with the interface cable.
  - If yes, the problem is in the cable.
  - If no, the problem is in the millimeter wave module.

The millimeter wave modules are not field repairable. Failed modules should be returned to your local service centers for repair. Or, they may be returned to:

Customer Service
Microwave Measurements Division
North American Measurements Group
Anritsu Company
490 Jarvis Drive
Morgan Hill, CA 95037-2809

If The Fault Is In The VNA

Generally, problems that occur in the VNA will cause the instrument to display error codes and be recorded to the Service Log.

However, since the VNA is the controller of the entire system, a problem occurring in another part of the system may also cause the VNA to generate an error message and record the failure to the service log.

DO NOT ASSUME THAT VNA ERROR CODE IS RELATED TO VNA PROBLEM.

One of example is the “6024 PHS LCK FAIL DE” error message. If a problem cuts off the signal sent to the a1 input during forward measurement (S11, S21) or the a2 input during reverse measurement (S12, S22), the VNA will display this 6024 error.

Refer to Chapter 5 of this manual for 371XXA problems.

E-11 SYSTEM DESCRIPTION

The system description is provided below.

System Overview

The 371XXA Millimeter Wave VNA system consists of four main component groups:

- Signal Sources
- Test Set
- Millimeter Wave Modules
- Vector Network Analyzer

Figure E-3 shows the 371XXA Millimeter Wave VNA system configuration and illustrates the interconnections between signal source, test

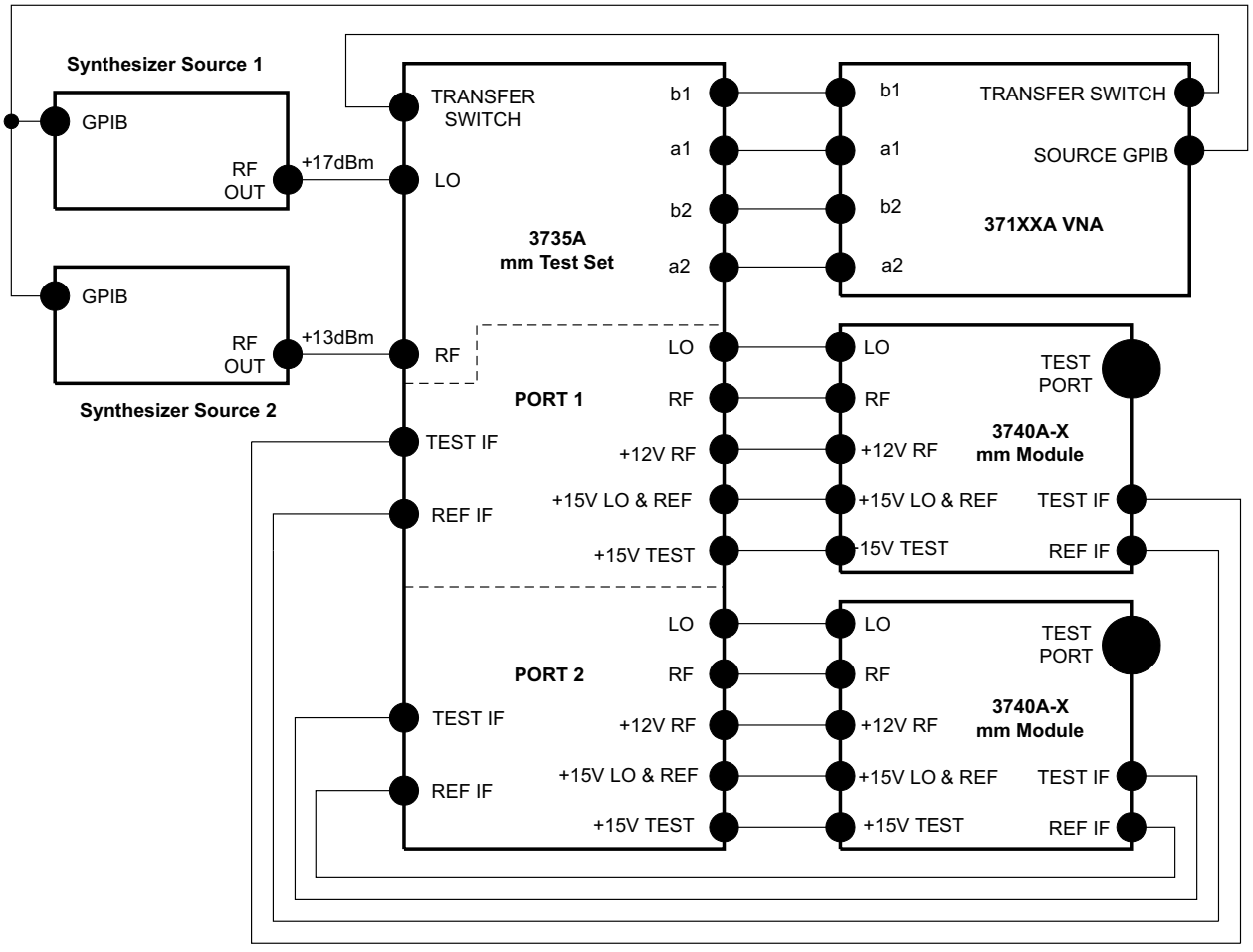


Figure E-3. 371XXA Millimeter Wave VNA System Interconnections

set, millimeter wave modules, and VNA. The following paragraphs contain brief descriptions of each system component groups.

Signal Sources Two Model 680XXC Synthesizers are used in the 371XXA Millimeter Wave VNA System. They are controlled by the 371XXA VNA via GPIB.

One 680XXC Synthesizer provides the LO drive signal for the system. It is used in 8 to 19 GHz frequency range and its power is set to +17 dBm. *Note:* Option 15 is required.

The other 680XXC Synthesizer is used to provide the RF drive signal for the system. It is used in 9 to 23 GHz frequency range and its power is set to +13 dBm. *Note:* Option 15 is required for this Source for F-Band operation.

Test Set The 3735B test set (Figures E-4 and E-5) contains the transfer switch, and a PCB Assembly which contains the power supply for the millimeter wave modules, and transfer switch and front panel LED's control logic circuitry.

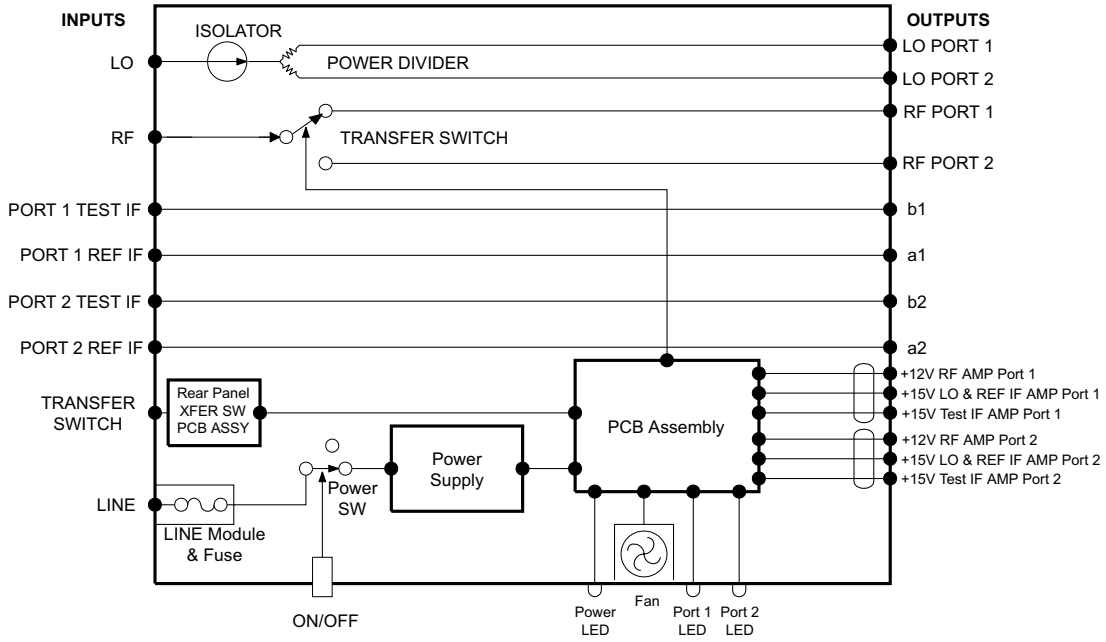


Figure E-4. 3735B Test Set Overall Block Diagram

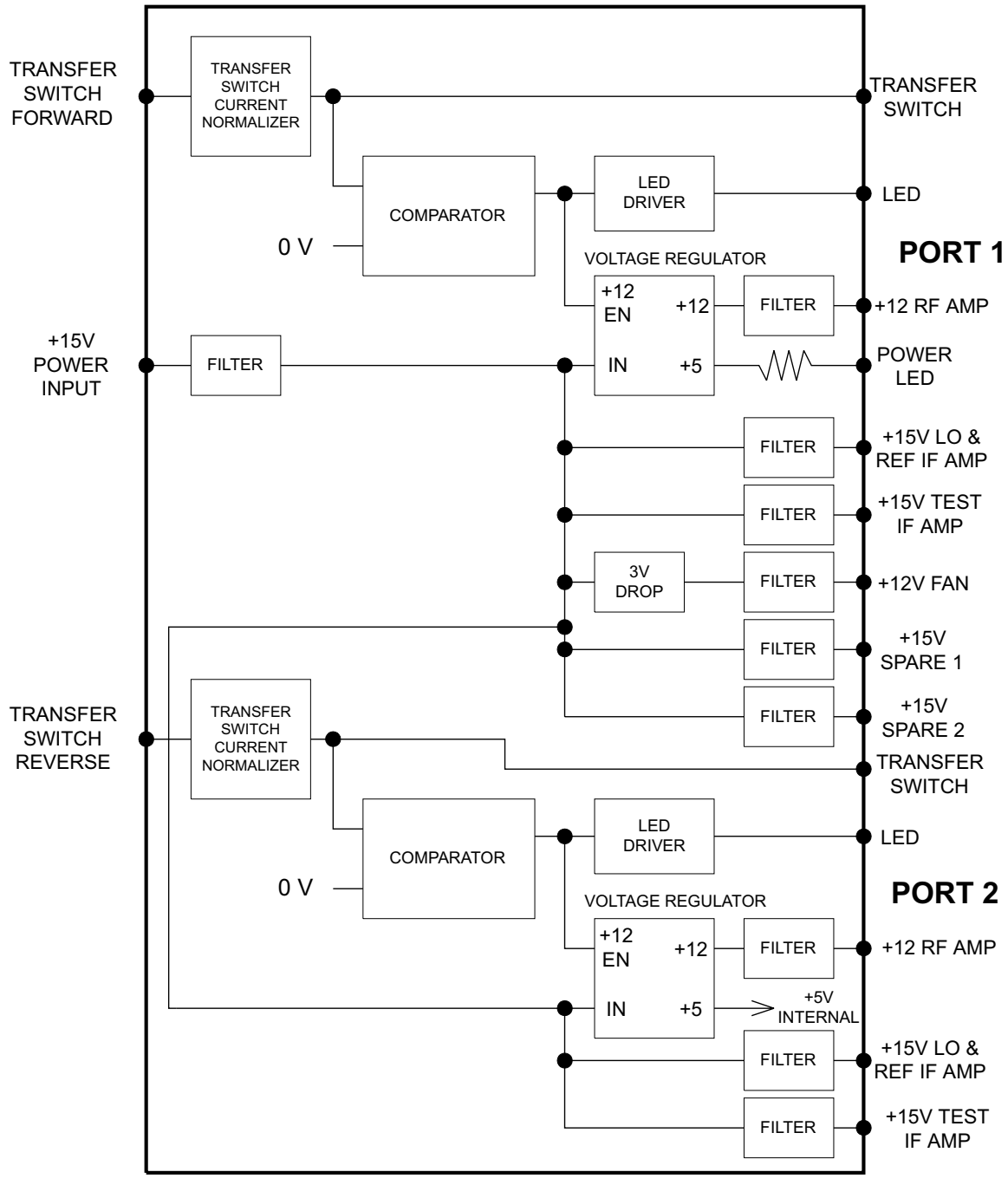
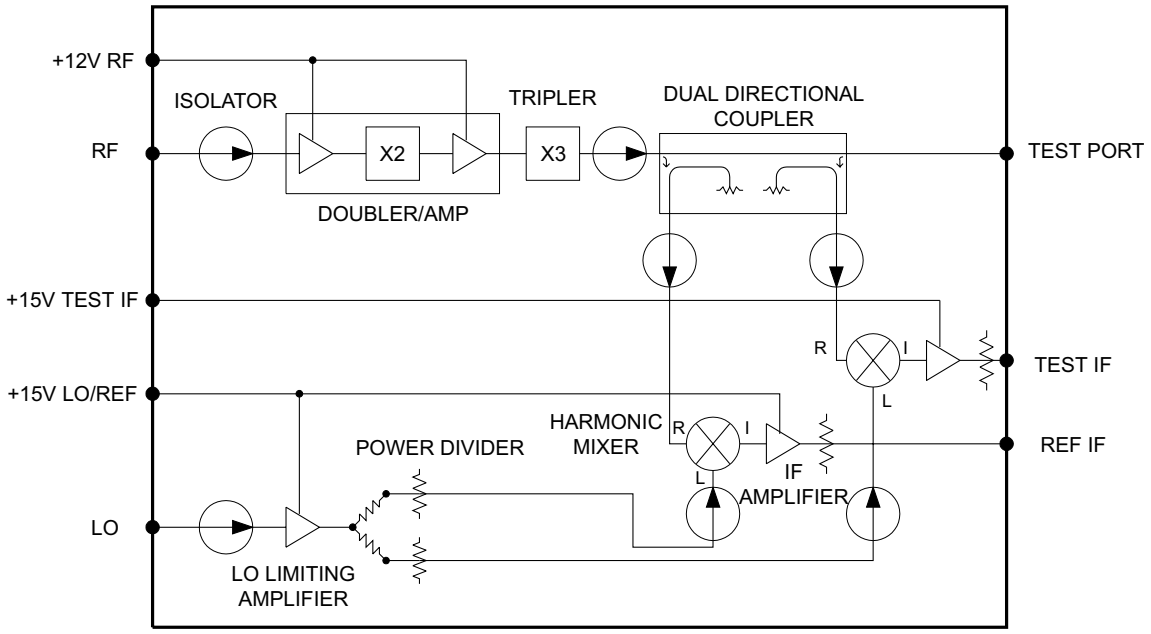


Figure E-5. *3735B Test Set PCB Assembly Block Diagram*

The RF drive signal from the synthesizer is switched in the test set using the transfer switch to provide RF to both the Port 1 and Port 2 millimeter wave modules.

Millimeter Wave Modules

The 3740A-X Millimeter Wave module (Figure E-6) contains the RF components to multiply the RF input to the desired test port frequency. E-, W-, and F-band modules use X2 and X3 multipliers. V-band module uses X2 and X2 multipliers. Q-band module uses X3 multiplier only.



NOTE:

WR-12 (E), WR-10 (W), & WR-8 (F) RF CHAIN SHOWN

WR-15 (V) = X2, X2; WR-22 (Q) = X3 ONLY

Figure E-6. *3740A-X Millimeter Wave Module Block Diagram*

Its also contains a dual directional coupler needed to make transmission and reflection measurements. Harmonic mixers are used to convert the Test and Reference signal from the coupler to the 270MHz Test and Reference IF signals that are sent to the VNA, via the test set.

The 3741A-X module contains the harmonic mixer necessary to generate the Test IF signal (Figure E-7). An external waveguide attenuator is used in conjunction with the 3741A-X.

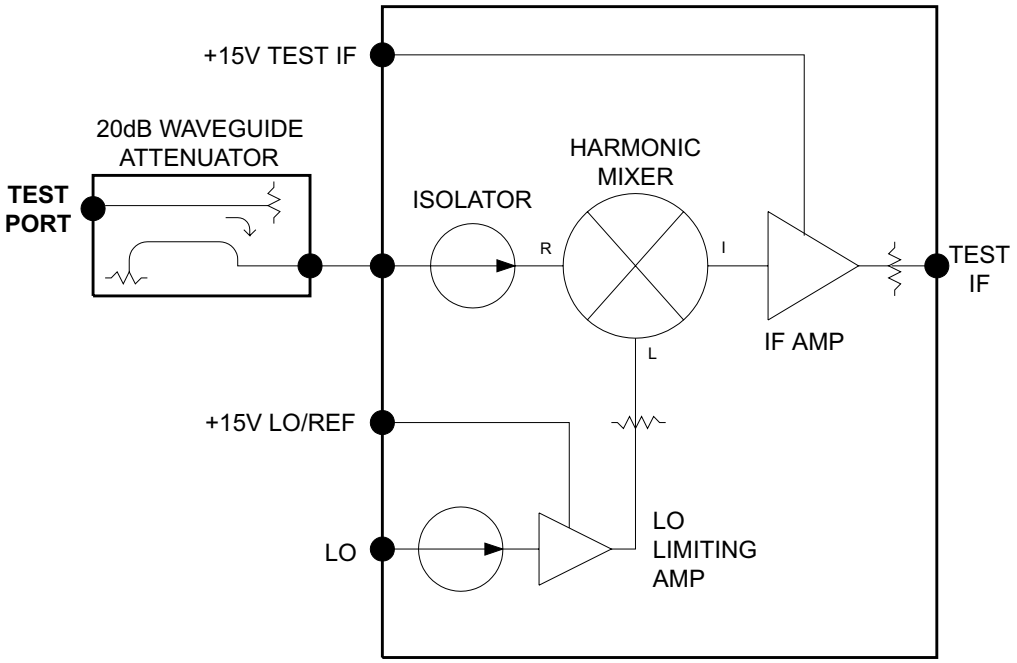


Figure E-7. *3741A-X Millimeter Wave Module Block Diagram*

Vector Network Analyzer

The 371XXA provides direct access to the four-channel sampler. The Test IF and Reference IF signals generated in the millimeter wave modules are sent to the four input a1, b1, a2, b2 of the VNA via the millimeter test set. The samplers are operated in direct (bypass) mode. The VNA is used in tracking mode and controls the two external synthesizers via the GPIB.

System Operation

The following paragraphs describe the operation of a 371XXA Millimeter Wave VNA System using the Model 3740A-E modules.

During a typical measurement, the RF Synthesizer, under the direct control of the VNA, outputs a RF signal to the test set. This RF signal is one-sixth (1/6) of the desired device-under-test (DUT) frequency.

This RF signal is switched in the test set using the transfer switch and is sent to the millimeter wave module through Port 1 or Port 2, depending on the S-parameter measured.

In the millimeter wave module, the RF signal is doubled and amplified in the Doubler/Amplifier and then tripled in the Tripler. The RF signal is then sent to the Test Port via the Coupler. This is the stimulus signal for the DUT. One coupled arm of the coupler provides the RF signal for the first harmonic mixer, generating the Reference IF signal.

When there is any impedance mismatch between the test port and the DUT input port, some of the signal incident at the DUT input port is reflected back to the test port of the millimeter wave module and some travels into the DUT. In the case of two port DUTs (that is those having an input and output port), the portion of the stimulus signal that travels through the DUT goes to the test port of the second millimeter wave module for measurement.

The reflected or transmitted test signal goes through the other coupled arm of the coupler and provides the RF signal for the second harmonic mixer, generating the Test IF signal.

The LO Synthesizer, under the direct control of the VNA, outputs a LO signal to the test set. This signal is one-fifth (1/5) of the desired DUT frequency offset by 270 MHz. The LO signal enters the millimeter wave module into a limiting amplifier, which is used to keep the LO power at a fixed level into the harmonic mixers. The LO signal is then split to provide inputs to both of the harmonic mixers.

The harmonic mixers, in the case of E band, use the fifth harmonic of the LO signal. In the first harmonic mixer, the fifth harmonic of the LO is mixed with the coupled off RF signal to create the 270 MHz Reference IF input to the VNA. In the second harmonic mixer, the fifth harmonic of the LO is mixed with the RF signal reflected or transmitted from the DUT creating the 270 MHz Test IF.

The Reference IF signal is sent to a1 or a2 input of the VNA. The Test IF signal is sent to b1 or b2 input of the VNA. In the case of S11 forward reflection measurement, Reference IF signal and Test IF signal from the Port 1 module are sent to a1 and b1 inputs of the VNA respectively.

Each of these IF signals carries embedded magnitude and phase information relative to a reference signal. In the VNA, they are converted to lower frequency IF signals. Down conversion of these signals does not affect the magnitude and phase relationship; only the frequency is changed. These converted IF signals are detected by the synchronous detectors of the VNA and then converted to digital data.

The VNA processors, controlled by embedded firmware coupled with system software, manipulate this digital data. Short-term system errors are normalized and digital compensation is generated and applied. The resultant S-Parameter data characterizing the DUT is then presented on the VNA color display, output to a printer or plotter, or routed to the rear panel external GPIB interface.

E-12 REMOVE AND REPLACE PROCEDURES (3735B TEST SET)

The Model 3735B Millimeter Wave Test Set consists of the replaceable subassemblies listed in Table E-1 and E-2 and shown in Figure E-1. These removal of these subassemblies is straight-forward and is described below. Refer to Figures E-8 and E-9 while reading the procedure. The replacement of the subassemblies is a reverse of the removal instructions.

Remove Covers

To remove top and bottom covers, proceed as follows:

Step 1. Remove the three screws from the rear of the top cover.

Step 2. Gently pry the cover loose from the rear panel, slide it to the rear and lift it off.

Step 3. Repeat steps 1 and 2 for the bottom cover.

NOTE

It is not necessary to remove the bottom cover, except to remove the two screws securing the power supply.

Remove Power Supply

To remove the Power Supply, proceed as follows:

Step 1. Remove the top and bottom covers (above).

Step 2. From the top, remove the plastic shield from the terminal strip.

Step 3. Remove the twisted-pair wires (1) from the top two terminals (+V and -V).

Step 4. Remove the line-voltage wires (2) from three bottom terminals: green-yellow wire from “ACG,” brown wire from “L,” and blue wire from “N.”

Step 5. While supporting the Power Supply with one hand, remove the two retaining screws from the underside with the other hand.

Step 6. Remove the Power Supply.

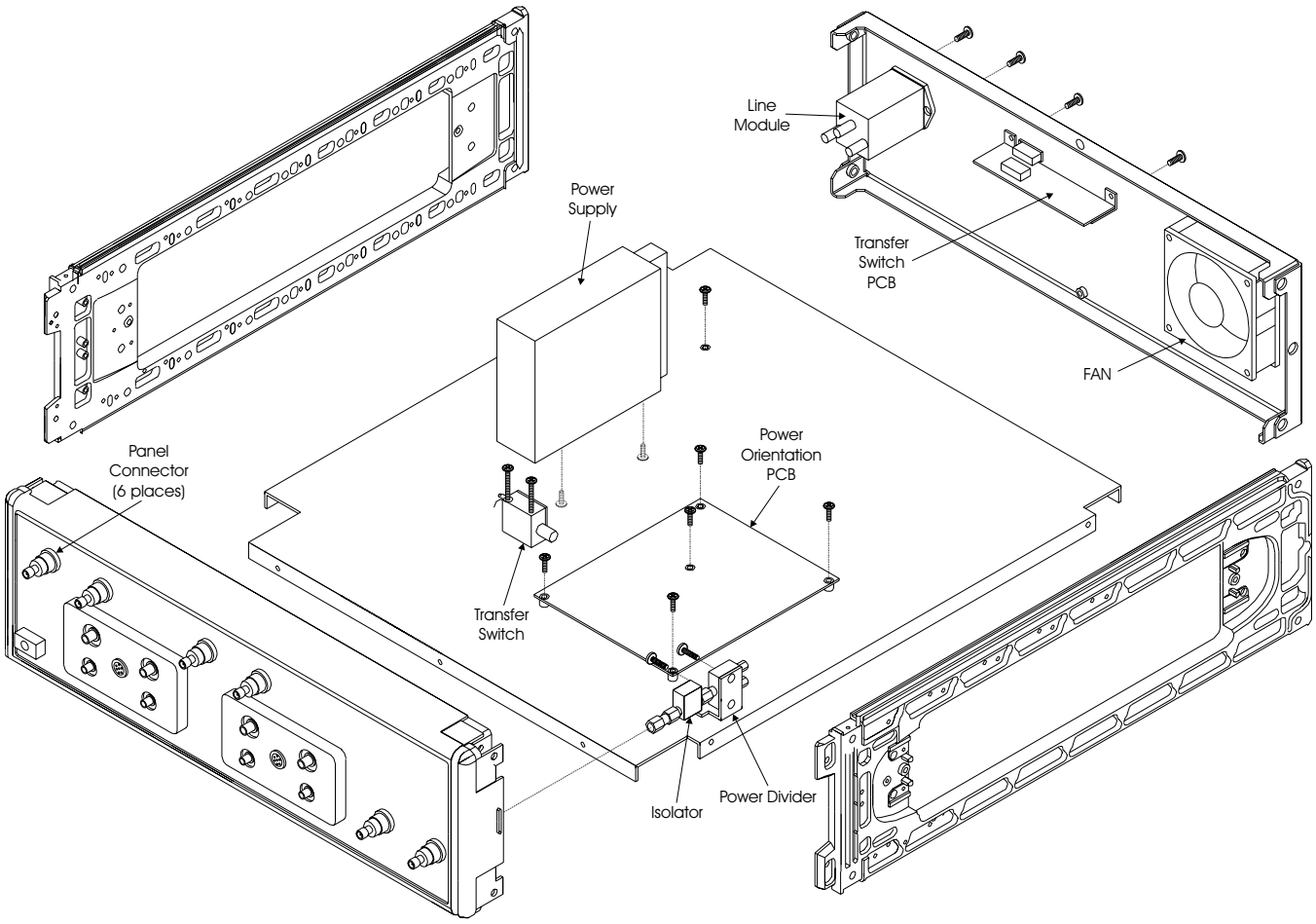


Figure E-8. *Replaceable Parts Exploded View*

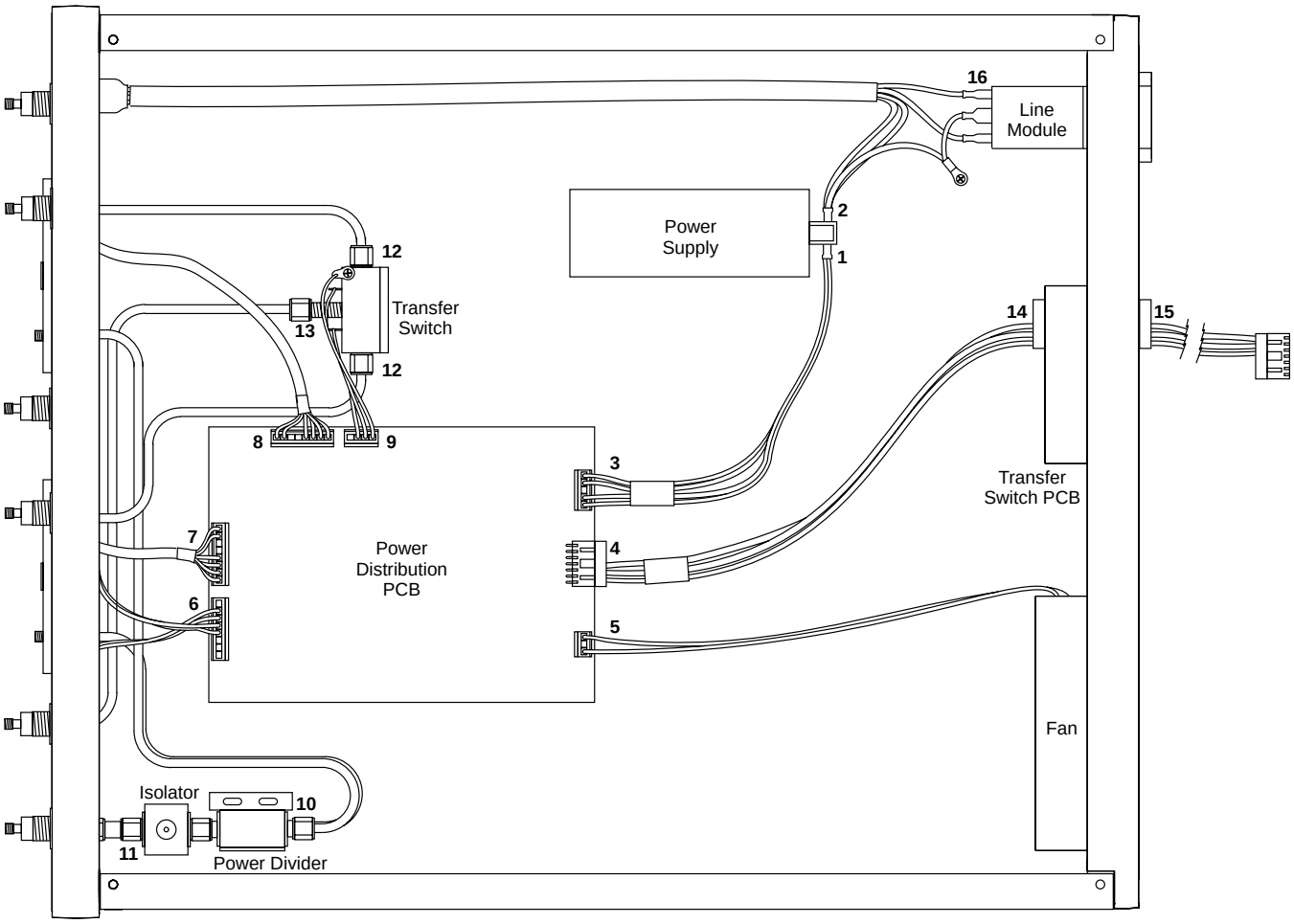


Figure E-9. *Wiring and Connectors on Replaceable Part (Keyed to Removal Procedures)*

Remove Power Distribution PCB

To remove the Power Distribution PCB, proceed as follows:

Step 1. Remove the top cover (above).

Step 2. Disconnect the seven plug-in connectors (3 through 9).

Step 3. Remove the five screws from the PCB.

Step 4. Lift the PCB straight up and away.

Remove Power Divide/Isolator Assembly

To remove the Power Divider and Isolator Assembly, proceed as follows:

Step 1. Remove the top cover (above).

Step 2. Disconnect the two connectors (10) from the rear of the Power Divider.

Step 3. Remove the two screws from the Power Divider.

Step 4. Disconnect the connector (11) on the front of the isolator.

Step 5. Remove the assembly.

Remove Transfer Switch Assembly

To remove the Transfer Switch Assembly, proceed as follows:

Step 1. Remove the top cover (above).

Step 2. Disconnect the two connectors (12) from the sides of the Transfer Switch.

Step 3. Remove the connector (13) from the front of the transfer switch.

Step 4. Remove the two screws from the top of the Transfer Switch.

Step 5. Remove the assembly.

Remove Transfer Switch PCB Assembly

To remove the Transfer Switch PCB, proceed as follows:

Step 1. Remove the top cover (above).

Step 2. Disconnect the two connectors; one from the inside of the unit (14) and the other from the outside (15) of the rear panel.

Step 3. Remove the two screws from the outside of the rear panel.

Step 4. Remove the assembly.

Remove Fan Assembly

To remove the Fan Assembly, proceed as follows:

Step 1. Remove the top cover (above).

Step 2. From the outside of the rear panel, remove the four thumb screws from the fan guard and remove the fan guard.

Step 3. Remove the connector from J5 (5) on the Power Distribution PCB.

Step 4. Remove the screws from the four corners and remove the Fan Assembly.

Remove Line Voltage Module

To remove the Line Voltage Module, proceed as follows:

Step 1. Remove the top cover (above).

Step 2. Remove the three push-on connectors (16) from the rear of the Line Voltage Module.

Step 3. Remove the two retaining screws from the outside of the rear panel.

Step 4. Remove the Line Voltage Module.

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